TDK InvenSense
ICM-45605 and ICM-45686
User Guide

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1 INTRODUCTION

The TDK InvenSense ICM-45605 and ICM-45686 User Guide is intended to be used as a companion document to ICM-45605 and ICM-45686 Product datasheet. It provides all the necessary details including register maps for all major product features and applications.

The ICM-45605 and ICM-45686 are dual interface device. ICM-45686 auxiliary interface has two functions, access sensor data through SPI slave interface and I^2C master. ICM-45605 auxiliary interface has I^2C master only.

The dual Interface device is a superset of single interface device. Please refer to individual part datasheet for interface details.

2 I²C MASTER USER GUIDE

Aux1 interface can be configured to I²C master for external sensor configuration and data accessing. Its operation is controlled through the host interface. The host can be an application processor connected to AP interface or the ICM-45605 and ICM-45686 built-in processor (eDMP).

2.1 I²CM (I²C MASTER) STRUCTURE

The function of I²CM is to convert read/write commands queued from the host (AP or eDMP) to external sensor I²C Slave transactions. Figure 1 shows how the I²CM function block works in the system.

Through the I²CM, the host can access up to two external sensors. The host sets the external sensor device slave address, writes register address and data, reads register start address, and executes commands.

The I²CM operation can be triggered by user-set external sensor ODR or by on-demand request from the host.

The I²CM function block is shown in Figure 1.

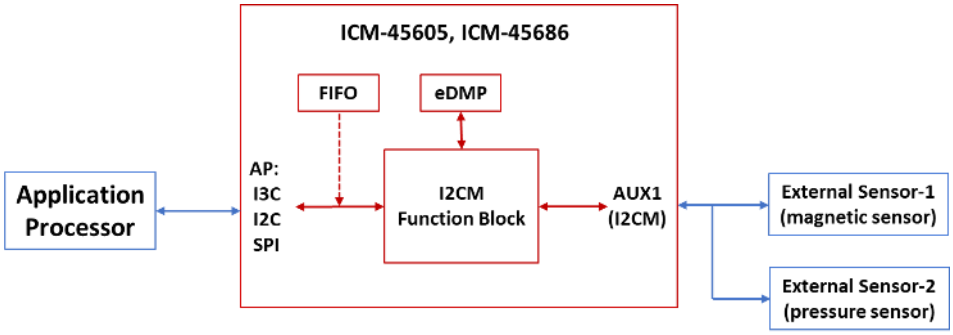


Figure 1. I²CM Functions

There is command buffer, device profile buffer, and write buffer which are programmed by the host with the required information for initiating I²C transactions with external sensor slave device. The read-out data from external sensors is stored in Read Buffer. The information contained in each buffer will be explained in the following sections.

In addition to Read Buffer, the received external sensor data can be reformatted by the eDMP. The reformatted external sensor data is then moved into FIFO along with other internal sensor data. The external host reads the FIFO to retrieve both the external sensor data and the internal sensor data.

Please refer to the datasheet to learn how to enable external sensor data to FIFO and the FIFO package data format.

The I²CM function block can be pass-through with register configuration. When the bitfield of AUX1_ENABLE_OVRD_VAL[3:2] is set to 2 in register IOC_PAD_SCENARIO_AUX_OVRD through AP interface, the AUX1 in I²CM bypass mode (when the host is not in SPI). Register IOC_PAD_SCENARIO can be read to confirm the changes made taken effect. When the I²CM is in pass-through mode, the host on AP interface can access external sensor directly.

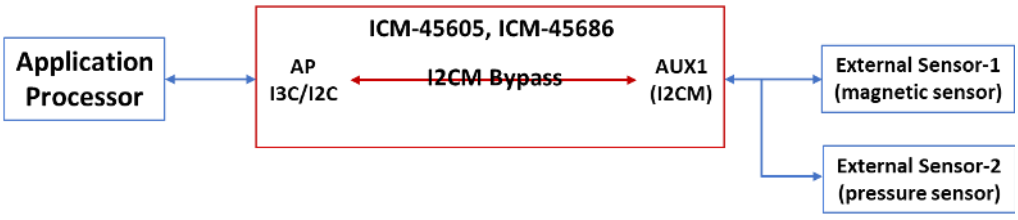


Figure 2. I²CM in Pass-Through

2.2 I²CM REGISTER SUMMARY

The following registers will be used for the I²CM configuration and execution. They are all accessed from the AP interface.

Name: IOC_PAD_SCENARIO
Bank: User bank 0
Address: 0x2F
Serial IF: R

BIT	NAME	FUNCTION
2:1	AUX1_MODE[1:0]	Effective only when 'AUX1_ENABLE' is '1' Selects modes at which AUX1 pads could be used 0: AUX1in SPI Slave 1: AUX1 in I2CM Master 2: AUX1 in I2CM Bypass (when host is not in SPI)
0	AUX1_ENABLE	AUX1 Enable 0: Disable 1: Enable

Name: IOC_PAD_SCENARIO_AUX_OVRD
Bank: User Bank 0
Address: 0x30

BIT	NAME	FUNCTION
4	AUX1_MODE_OVRD	Override enable for AUX1_MODE 0: Disable 1: Enable
3:2	AUX1_ENABLE_OVRD_VAL	Override value: Effective only when 'AUX1_ENABLE' is '1' Selects modes at which AUX1 pads could be used 0: AUX1in SPI Slave 1: AUX1 in I2CM Master 2: AUX1 in I2CM Bypass (Enable only when AP is not in SPI mode) NOTE: When enabling the I2CM bypass, this register should be programmed individually, not a part of a burst transaction.
1	AUX1_ENABLE_OVRD	Override enable for AUX1_ENABLE 0: Disable 1: Enable
0	AUX1_ENABLE_OVRD_VAL	Override value for AUX1 enable: 0: AUX1 disabled 1: AUX1 enabled

There are four command buffer registers, I2CM_COMMAND_0~3. Their bit fields and functions are same. I2CM_COMMAND_0 is explained here only.

Name: I2CM_COMMAND_0
Bank: IPREG_TOP1
Address: 0x06

BIT	NAME	FUNCTION
7	ENDFLAG_0	1: Indicates the current entry is the last I²C communication with the external slave device.
6	CH_SEL_0	Specify the channel for transaction

5:4	R_W_0[1:0]	R/W command. 0: for Write Op. 1: for Read Op with register address specified. 2: for Readd Op without register address specified.
3:0	BURSTLEN_0[3:0]	Specifies the burst length of I2C communication with the external slave device.

Name: I2CM_DEV_PROFILE0
Bank: IPREG_TOP1
Address: 0x0E

BIT	NAME	FUNCTION
7:0	RD_ADDRESS_0[7:0]	Specifies the read address for the channel 0 I2C transaction

Name: I2CM_DEV_PROFILE1
Bank: IPREG_TOP1
Address: 0x0F

BIT	NAME	FUNCTION
6:0	DEV_ID_0[6:0]	Specifies the slave ID for the channel 0 I2C transaction

Name: I2CM_DEV_PROFILE2
Bank: IPREG_TOP1
Address: 0x10

BIT	NAME	FUNCTION
7:0	RD_ADDRESS_1[7:0]	Specifies the read address for the channel 1 I2C transaction

Name: I2CM_DEV_PROFILE3
Bank: IPREG_TOP1
Address: 0x11

BIT	NAME	FUNCTION
6:0	DEV_ID_1[6:0]	Specifies the slave ID for the channel 1 I2C transaction

There are six write buffer registers, I2CM_WR_DATA0 ~ 5. Their bit fields and functions are same. I2CM_WR_DATA0 is explained here only.

Name: I2CM_WR_DATA0
Bank: IPREG_TOP1
Address: 0x33

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA0[7:0]	The data/address byte for a Write transaction

There are 21 read buffer registers, I2CM_RD_DATA0 ~ 20. Their bit fields and functions are same. I2CM_RD_DATA0 is explained here only. Received external sensor data will be saved in I2CM_RD_DATA0 ~ 20 sequentially.

Name: I2CM_RD_DATA0
Bank: IPREG_TOP1

Address: 0x1B		
BIT	**NAME**	**FUNCTION**
7:0	I2CM_RD_DATA0[7:0]	The first byte received from i2c slave.

Name: DMP_EXT_SEN_ODR_CFG Bank: User bank0 Address: 0x27		
BIT	**NAME**	**FUNCTION**
6	EXT_SENSOR_EN	Enable generating the ODR event for external sensor operation per the setting of ext_odr register. 0: Disable 1: Enable
5:3	EXT_ODR[2:0]	I^2CM external sensor ODR to kick off I^2CM operation 000: 3.125 Hz 001: 6.25 Hz 010: 12.5 Hz 011: 25 Hz 100: 50 Hz 101: 100 Hz 110: 200 Hz 111: 400 Hz

Name: I2CM_CONTROL Bank: IPREG_TOP1 Address: 0x16		
BIT	**NAME**	**FUNCTION**
6	I2CM_RESTART_EN	0x0: No Restart is used. Default is 0. 0x1: if R/W=1, the Restart is used to bridge the register-address write transaction and register-data read transaction. This bit is not programmable by MCU when i2cm_busy = 1.
3	I2CM_SPEED	0: I2C Fast Mode. Default is 0. 1: I2C Standard Mode. This bit is not programmable by MCU when i2cm_busy = 1.
0	I2CM_GO	1: Kicks off I2C master operation. Clears to 0 after I2C master operation is completed. This bit is not programmable when I2CM_BUSY = 1

Name: I2CM_STATUS Bank: IPREG_TOP1 Address: 0x18		
BIT	**NAME**	**FUNCTION**
5	I2CM_SDA_ERR	SDA Error Indication
4	I2CM_SCL_ERR	SCL Error Indication

3	I2CM_SRST_ERR	SRST Error Indication
2	I2CM_TIMEOUT_ERR	Timeout Indication
1	I2CM_DONE	I^2CM done Indication
0	I2CM_BUSY	I^2CM busy Indication

Name: I2CM_EXT_DEV_STATUS
Bank: IPREG_TOP1
Address: 0x1A

BIT	NAME	FUNCTION
3:0	I2CM_EXT_DEV_STATUS[3:0]	status tracks the ACK/NACK feedback from the external device per each entry of the command buffer. 1=NACK, 0=ACK

NameINT_I2CM_SOURCE
Bank: IPREG_TOP1
Address: 0x74

BIT	NAME	FUNCTION
1	INT_STATUS_I2CM_SMC_EXT_ODR_EN	For i2cm interface, enable interrupt status bit to flag the occurrences of smc_ext_odr event. 1: Source enabled. 0: Source disabled.
0	INT_STATUS_I2CM_IOC_EXT_TRIG_EN	For i2cm interface, enable interrupt status bit to flag the occurrences of ioc_ext_trg event. 1: Source enabled. 0: Source disabled.

Name: REG_MISC1
Bank: UserBank0
Address: 0x35

BIT	NAME	FUNCTION
3:0	OSC_ID_OVRD[3:0]	Must be 1 or 2 (if gyro is enabled) for I2CM operation.

3 FIFO

ICM-45605 and ICM-45686 contains up to 8 KB of FIFO. 2 KB of default FIFO and it can be extended to 8 KB by disabling APEX.

3.1 INTERNAL SENSORS PACKET STRUCTURES

FIFO packets are assembled in different packet sizes based on the enabled sensors. When internal sensors Accel and Gyro are enabled, the following packets are available:

- 8 -byte packet: Contains Header Accel-only or Gyro-only data and Temperature data (1 byte)
- 16-byte packet: Contains Header Accel data, Gyro data, Temperature data (1 byte), Timestamp
- 20-byte packet: Contains high-resolution Accel data(19bits), Gyro data(20bits), Temperature data (2 bytes), Timestamp

3.2 EXTERNAL SENSORS PACKET STRUCTURES

If external sensors ES0 and ES1 are enabled for FIFO, the following packets are available.

- 16-byte packet: Contains 2 Bytes Header 6/9 bytes ES0-only or ES1-only data
- 20-byte frame: Contains 2 Bytes Header 6/9 bytes ES0 data and ES1 data
- 32-byte frame: Contains 2 Bytes Header Accel data, Gyro data, 6/9 bytes ES0 data, ES1 data, Temperature data (1 byte), Timestamp.

The 32 bytes format is always selected when at least one internal sensor and one external sensor are enabled.

3.3 FIFO COMPRESSION

FIFO Compression algorithm allows to send compressed sensor data into FIFO frames reducing the number of stored frames, thus virtually providing more FIFO space. It allows the storage of up to 4 times the number of frames with respect to the non-compressed standard flow. Frame decompression oversees the host, which reads the FIFO.

Compression uses a hardware lossless algorithm, based on data variation analysis of each axis. The differences between two consecutive 16-bit samples of each axis is analyzed. Small differences can be stored using less bits.

The supported compression ratios are as follows:

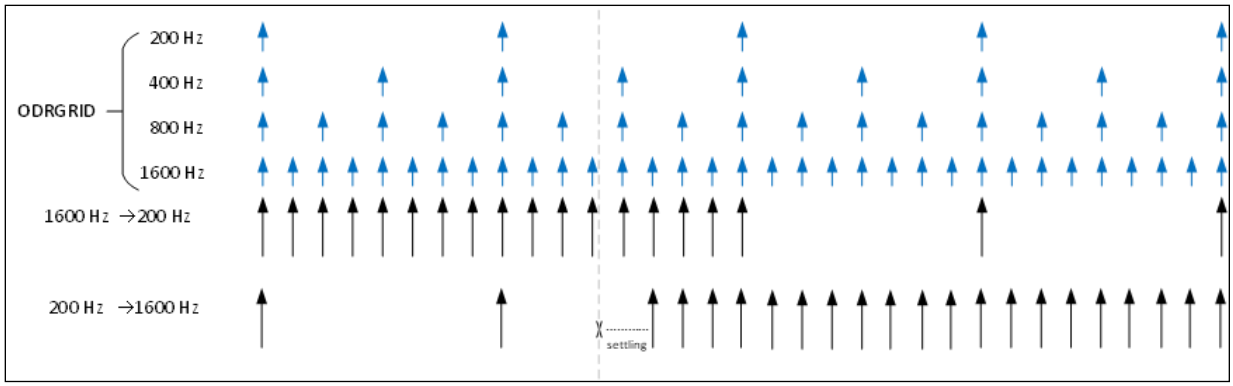
- x1 (non-compressed reference frame): the difference between the current and previous data is higher than 128 LSB
- x2: the difference between the current and previous data is between 16 LSB and 128 LSB → Axes are represented with 8 bits signed data
- x3: the difference between the current and previous data is between 8 LSB and 16 LSB → Axes are represented with 5 bits signed data
- x4: the difference between the current and previous data is less than 8 LSB → Axes are represented with 4 bits signed data

3.4 FIFO POINTS TO CONSIDER

3.4.1 Dynamic ODR Changing

Dynamic change in ODR from ODR A to ODR B, following 2 cases are possible

ODR A faster than ODR B:
Change to ODR B will be effective after few ODR A.
ODR A slower than ODR B:
After the change from A to B, the ODR will be between A and B to let ODR B settle to its accurate value.



In above figure dotted line is where ODR change command is issued.
In case of 1600Hz to 200Hz we see few samples at 1600Hz and then settles at 200Hz.
In case of 200Hz to 1600Hz we see settling time and then it is at 1600Hz.

3.4.2 FIFO_IF to be set at last

FIFO_IF must be enable at end of setting up the FIFO. FIFO should be in bypass mode while setting up watermark threshold, frame format and FIFO mode. Once all setup is done, we enable FIFO_IF bit.
With FIFO enabled, fifo_if enabled and sensor enabled, but without mapping accel and gyro data to FIFO, the FIFO count will still increase, and the FIFO watermark will still be generated.

3.5 SETTING UP FIFO

The following configuration sets up the FIFO.

Field Name	Register Name	Register Address(bit)	Bank	Value	Description
FIFO_HIRES_EN	FIFO_CONFIG3	0x21 (3)	Bank 0	0	Disable All FIFO.
FIFO_GYRO_EN		0x21 (2)		0	
FIFO_ACCEL_EN		0x21(1)		0	
FIFO_IF_EN		0x21(0)		0	
INT1_STATUS_EN_FIFO_THS	INT1_CONFIG0	0x16(1)	Bank 0	1	Enable FIFO Threshold interrupt
FIFO_MODE	FIFO_CONFIG0	0x1D(7:6)	Bank 0	0	FIFO Disabled
TMST_EN	SMC_CONTROL_0	0x58(1)	IPREG_TOP1	1	Timestamp Enable for FIFO
FIFO_WM_TH[7:0]	FIFO_CONFIG1_0	0x1E(7:0)	Bank 0	0xA0	FIFO Watermark to threshold. In this example 0xA0.
FIFO_WM_TH[15:8]	FIFO_CONFIG1_1	0x1F(7:0)		0	FIFO Watermark to be hit MSB. In this example 0x00.
FIFO_WR_WM_GT_TH	FIFO_CONFIG2	0x20(3)	Bank 0	1	Write watermark interrupt generated when FIFO data count is greater than or equal to FIFO watermark threshold
FIFO_GYRO_EN	FIFO_CONFIG3	0x21(2)	Bank 0	1	Enable Gyro
FIFO_ACCEL_EN		0x21(1)		1	Enable Accel
FIFO_MODE[1:0]	FIFO_CONFIG0	0x1D(7:6)	Bank 0	1	FIFO Stream Mode Enable
FIFO_IF_EN	FIFO_CONFIG3	0x21 (0)	Bank 0	1	Enable FIFO

3.6 SETTING UP FIFO FOR EXTERNAL SENSOR

Field Name	Register Name	Register Address(bit)	Bank	Value	Description
INT1_STATUS_EN_FIFO_THS	INT1_CONFIG0	0x16(1)	Bank 0	1	Enable FIFO Threshold interrupt
FIFO_MODE[1:0]	FIFO_CONFIG0	0x1D(7:6)	Bank 0	0	FIFO Disabled
TMST_EN	SMC_CONTROL_0	0x58(1)	IPREG_TOP1	1	Timestamp Enable for FIFO
FIFO_WM_TH[7:0]	FIFO_CONFIG1_0	0x1E(7:0)	Bank 0	0xA0	FIFO Watermark to be hit LSB. In this example 0xA0.
FIFO_WM_TH[15:8]	FIFO_CONFIG1_1	0x1F(7:0)	Bank 0	0	FIFO Watermark to be hit MSB. In this example 0x00.
FIFO_WR_WM_GT_TH	FIFO_CONFIG2	0x20(3)	Bank 0	1	Write watermark interrupt generated when FIFO data count is greater than or equal to FIFO watermark threshold
FIFO_ES0_EN	FIFO_CONFIG3	0x21(4)	Bank 0	1	Enable External Sensor 0
FIFO_ES1_EN		0x21(5)		1	Enable External Sensor 1
FIFO_ES0_6B_9B	FIFO_CONFIG4	0x22(0)	Bank 0	1	External Sensor 0 size is 9 bytes
FIFO_MODE[1:0]	FIFO_CONFIG0	0x1D(7:6)	Bank 0	1	FIFO Stream Mode Enable
FIFO_IF_EN	FIFO_CONFIG3	0x21 (0)	Bank 0	1	Enable FIFO

4 APEX USER GUIDE

4.1 APEX OVERVIEW

The ICM-45605 and ICM-45686 natively supports a series of motion algorithms. For this purpose, it embeds a proprietary core (eDMP) along with 16 KB of ROM and 8 KB of SRAM.

The following APEX features are implemented in the ROM:

Pedometer
SMD
Tilt
Raise to Wake/Sleep
LowG
HighG
Freefall
Tap
WOM

The 8 KB SRAM is shared among data memory allocated for the ROM features, the stack, and the FIFO. Data memory usage for ROM features is 1280 bytes, leaving 6192 bytes for the stack and the FIFO.

Pedometer: Tracks Step Count, also issues Step Detect interrupt.

Significant Motion Detection: Detects significant motion based on accelerometer data.

Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35° for more than a programmable time.

Raise to Wake/Sleep: Gesture detection for wake and sleep events. Interrupt is issued when either of these two events are detected.

LowG Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.

HighG Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.

Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.

Single Tap / Double Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.

Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold.

4.2 APEX RELATED REGISTERS

4.2.1 Host direct vs indirect access register

All “USER BANK 0” registers are accessible directly from the host through serial interface using the register address given in following table.

All other register banks including IMEM_SRAM are indirect access registers (IREG), not accessible directly by a 7-bit address on serial interface. IREGs can only be accessed through a dedicated procedure using an internal 16-bit address given in the following table. For the details of IREGs access procedure, refer to the datasheet.

4.2.2 Configuration registers

Reg. Bank	Register Name	Addr	Bit Field	Functionality
USER BANK 0	ACCEL_CONFIG0	0x1B	ACCEL_ODR[3:0]	Accelerometer Output Data Rate at the UI/AP FIFO.
	APEX_BUFFER_MGMT	0x2B	FF_DURATION_HOST_RPTR[1:0]	LSB indicates SRAM address for host to read MSB indicates size 2 buffer wrap around 00: host reads buffer 0 01: host reads buffer 1 10: host reads buffer 0 11: host reads buffer 1
			FF_DURATION_EDMP_WPTR[1:0]	LSB indicates SRAM address for eDMP to write MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1
	DMP_EXT_SEN_ODR_CFG	0x27	APEX_ODR[2:0]	Internal external ODR for I2CM kickoff 000: 3.125 Hz 001: 6.25 Hz 010: 12.5 Hz 011: 25 Hz 100: 50 Hz 101: 100 Hz 110: 200 Hz 111: 400 Hz
	EDMP_APEX_EN0	0x29	TAP_EN	Set 1 to enable Tap algorithm
			TILT_EN	Set 1 to enable Tilt algorithm
			PEDO_EN	Set 1 to enable pedometer algorithm
			FF_EN	Set 1 to enable Freefall algorithm
			R2W_EN	Set 1 to enable Raise to Wake algorithm
			SMD_EN	Set 1 to enable SMD algorithm
	EDMP_APEX_EN1	0x2A	INIT_EN	This bit is set by the host to indicate: eDMP executes only the segment of code that initialize constants used by algorithms. The register is R/W by the external host through the direct register accessing path. The register is R/C by any AHB master when it is accessed via internal AHB/APB bus.
			EDMP_ENABLE	Set 1 to enable eDMP
			POWER_SAVE_EN	Set 1 to enable power save mode
	REG_HOST_MSG	0x73	EDMP_ON_DEMAND_EN	Set 1 to create pulse to set int_status_edmp_on_demand_pin_0, int_status_edmp_on_demand_pin_1, Int_status_edmp_on_demand_pin_2 to 1

IPREG_TOP1	SMC_CONTROL_0	0x58	ACCEL_LP_CLK_SEL	
	EDMP_PRGRM_IRQ0_0	0x4F		start address of IRQ_0 vector
	EDMP_PRGRM_IRQ0_1	0x50		start address of IRQ_0 vector
	EDMP_PRGRM_IRQ1_0	0x51		start address of IRQ_1 vector
	EDMP_PRGRM_IRQ1_1	0x52		start address of IRQ_1 vector
	EDMP_PRGRM_IRQ2_0	0x53		start address of IRQ_2 vector
	EDMP_PRGRM_IRQ2_1	0x54		start address of IRQ_2 vector
	EDMP_SP_START_ADDR	0x55		bit [15:8] of AHB address of SRAM allocated for DMP stack
	FIFO_SRAM_SLEEP	0xA7	FIFO_GSLEEP_SHARED_SRAM	Set selected SRAM bank global sleep mode (pwr_gsleep) 0: selected SRAM bank sleep mode is controlled by PSEQ, ps_fifo_gsleep_fifo_sram if this bank contains FIFO data. Otherwise, SRAM is in sleep mode (SRAM bank pwr_gsleep=1). 1: selected SRAM bank remains in active mode (pwr_gsleep=0). Can be changed when FIFO is disabled (Bypass mode), AHB interface idle.
	STATUS_MASK_PIN_0_7	0x71	INT_ON_DEMAND_PIN_0_DIS	For irq0, on-demand drdy event, this is to enable the interrupt pin assertion when the int_status_on_demand_drdy status bit is 1. 1: No Interrupt pin assertion. 0: enable the Interrupt pin assertion.
			INT_ACCEL_DRDY_PIN_0_DIS	For irq0, accel drdy event, this is to enable the interrupt pin assertion when the int_status_accel_drdy status bit is 1. 1: No Interrupt pin assertion. 0: enable the Interrupt pin assertion.
	IPREG_MISC	0x97	EDMP_IDLE	1: Indicates eDMP is idle 0 : Indicates eDMP is busy
IPREG_SYS2	IPREG_SYS2_REG_129	0x81	ACCEL_LP_AVG_SEL	Accel Low Power Mode Average Selection 0:1 1:2 2:4 3:5 4:7 5:8 6:10 7:11 8:16 9:18 10:20 11 :32 12-15: 64
	IPREG_SYS2_REG_131	0x83	ACCEL_UI_LPFBW_SEL	Selects UI path low pass cut-off 0:bypass; 1: ODR/4 2: ODR/8 3:ODR/16 4:ODR/32 5:ODR/64 6,7:ODR/128

4.2.3 APEX algorithms parameter registers

4.2.3.1 Power saving control

Reg. Bank	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_196 POWER_SAVE_TIME[7:0]	0xC4	1	Time of inactivity after which eDMP goes in power save mode Unit: Time in sample number Range: [0 – 4294967295] Default: 6400 corresponding to 8s for ODR = 800Hz
	IMEM_SRAM_REG_197 POWER_SAVE_TIME[8:15]	0xC5	1	
	IMEM_SRAM_REG_198 POWER_SAVE_TIME[16:23]	0xC6	1	
	IMEM_SRAM_REG_199 POWER_SAVE_TIME[24:31]	0xC7	1	

4.2.3.2 Pedometer parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_1008 PED_AMP_TH[7:0]	0x3F0	1	Threshold of step detection sensitivity. Low values increase detection sensitivity: reduce miss-detection. High values reduce detection sensitivity: reduce false-positive. Unit: g in q25. Range: [1006632 - 3019898] Default: 2080374
	IMEM_SRAM_REG_1009 PED_AMP_TH[15:8]	0x3F1	1	
	IMEM_SRAM_REG_1010 PED_AMP_TH[23:16]	0x3F2	1	
	IMEM_SRAM_REG_1011 PED_AMP_TH[31:24]	0x3F3	1	
	IMEM_SRAM_REG_988 PED_STEP_CNT_TH[7:0]	0x3DC	1	Minimum number of steps that must be detected before step count is incremented. Low values reduce latency but increase false positives. High values increase step count accuracy but increase latency Unit: Number of steps Range: [0-15] Default: 5
	IMEM_SRAM_REG_989 PED_STEP_CNT_TH[15:8]	0x3DD	1	
	IMEM_SRAM_REG_990 PED_STEP_DET_TH[7:0]	0x3DE	1	Minimum number of steps that must be detected before step event is signaled. Low values reduce latency but increase false positives. High values increase step event validity but increase latency. Unit: number of steps Range: [0-7] Default: 2
	IMEM_SRAM_REG_991 PED_STEP_DET_TH[15:8]	0x3DF	1	
	IMEM_SRAM_REG_994 PED_SB_TIMER_TH[7:0]	0x3E2	1	Duration before algorithm considers that user has stopped taking steps. Unit: time in samples number Range: [0 - 225] Default: 150 for ODR = 50Hz
	IMEM_SRAM_REG_995 PED_SB_TIMER_TH[15:8]	0x3E3	1	
	IMEM_SRAM_REG_1016 PED_HI_EN_TH[7:0]	0x3F8	1	Threshold to classify acceleration signal as motion not due to steps High values improve vibration rejection. Low values improve detection. Unit: g in q25. Range: [2949120 - 5210112] Default: 3506176
	IMEM_SRAM_REG_1017 PED_HI_EN_TH[15:8]	0x3F9	1	
	IMEM_SRAM_REG_1018 PED_HI_EN_TH[23:16]	0x3FA	1	
	IMEM_SRAM_REG_1019 PED_HI_EN_TH[31:24]	0x3FB	1	
	IMEM_SRAM_REG_1004	0x3EC	1	Pedometer sensitivity mode.

	PED_SENSITIVITY_MODE			Slow walk mode improves slow walk detection (<1 Hz) but the number of false positives may increase Range: 0: Normal 1: Slow walk Default: 0
	IMEM_SRAM_REG_1000 PED_LOW_EN_AMP_TH[7:0]	0x3E8	1	Threshold to select a valid step. Used to increase step detection for slow walk use case only. Unit: g in q25. Range: [1006632 - 3523215] Default: 2684354
	IMEM_SRAM_REG_1001 PED_LOW_EN_AMP_TH[15:8]	0x3E9	1	
	IMEM_SRAM_REG_1002 PED_LOW_EN_AMP_TH[23:16]	0x3EA	1	
	IMEM_SRAM_REG_1003 PED_LOW_EN_AMP_TH[31:24]	0x3EB	1	

4.2.3.3 SMD parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_1042 SMD_SENSITIVITY	0x412	1	Parameter to tune SMD algorithm robustness to rejection, ranging from 0 to 4 (values higher than 4 are reserved). Low values increase detection rate but increase false positives. High values reduce false positives but reduce detection rate (especially for transport use cases). Unit: N/A Ranging: [0 - 4] Default: 0

4.2.3.4 Tilt parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_392 TILT_WAIT_TIME[7:0]	0x188	1	Minimum duration for which the device should be tilted before signaling event. Unit: time in sample number Range: [0 - 65536] Default: 200 for ODR = 50Hz, 100 for ODR = 25Hz
	IMEM_SRAM_REG_393 TILT_WAIT_TIME[15:8]	0x189	1	
	IMEM_SRAM_REG_146 TILT_RESET_EN	0x92	1	Set 1 to reset tilt prior to any further tilt processing on next sensor data. Unit: N/A Range: [0 - 1] Default: 0
	IMEM_SRAM_REG_92 QUAT_RESET_EN	0x5C	1	Set 1 to force reset 3-axis quaternion when next tilt reset is done. This is applicable only if tilt_reset_en is also set to 1. Unit: N/A Range: [0 – 1] Default: 0

4.2.3.5 R2W parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_540 R2W_SLEEP_TIME_OUT[7:0]	0x21C	1	Defines the duration after wake event to report sleep event no matter if position changes or not. Unit: time in ms (millisecond) Range: [100 - 10000] Default: 640 (equivalent to 0.64s)
	IMEM_SRAM_REG_541 R2W_SLEEP_TIME_OUT[15:8]	0x21D	1	
	IMEM_SRAM_REG_542 R2W_SLEEP_TIME_OUT[23:16]	0x21E	1	
	IMEM_SRAM_REG_543 R2W_SLEEP_TIME_OUT[31:24]	0x21F	1	
	IMEM_SRAM_REG_544 R2W_SLEEP_GESTURE_DELAY[7:0]	0x220	1	Defines the minimal duration of sleep position before trigger the sleep event. Unit: time in ms (millisecond) Range: [0 - 256] Default: 96 (equivalent to 0.096s)
	IMEM_SRAM_REG_545 R2W_SLEEP_GESTURE_DELAY[15:8]	0x221	1	
	IMEM_SRAM_REG_546 R2W_SLEEP_GESTURE_DELAY[23:16]	0x222	1	
	IMEM_SRAM_REG_547 R2W_SLEEP_GESTURE_DELAY[31:24]	0x223	1	
	IMEM_SRAM_REG_548 R2W_MOUNTING_MATRIX[7:0]	0x224	1	Mounting matrix to rotate data from chip frame to device frame. Unit: N/A Range: 3 lower bits only are used [b2 b1 b0]: b2 = 1 swap X and Y b1 = 1 flip X sign b0 = 1 flip Y sign Default: 0 (chip frame aligned with android frame)
	IMEM_SRAM_REG_549 R2W_MOUNTING_MATRIX[15:8]	0x225	1	
	IMEM_SRAM_REG_550 R2W_MOUNTING_MATRIX[23:16]	0x226	1	
	IMEM_SRAM_REG_551 R2W_MOUNTING_MATRIX[31:24]	0x227	1	
	IMEM_SRAM_REG_556 R2W_GRAVITY_FILTER_GAIN[7:0]	0x22C	1	Gain used to filter the accelerometer to obtain an estimation of the gravity (low-pass filter), defined as: forgetting factor = Gain * SAMPLING_PERIOD / (40 * 32), and 100Hz. Range: [2-16] Default: 6 for ODR = 50Hz, 8 for ODR = 25Hz
	IMEM_SRAM_REG_557 R2W_GRAVITY_FILTER_GAIN[15:8]	0x22D	1	
	IMEM_SRAM_REG_558 R2W_GRAVITY_FILTER_GAIN[23:16]	0x22E	1	
	IMEM_SRAM_REG_559 R2W_GRAVITY_FILTER_GAIN[31:24]	0x22F	1	
	IMEM_SRAM_REG_560 R2W_MOTION_THR_ANGLE_COSINE[7:0]	0x230	1	Set the minimal angle that needed to be applied to device to detect R2W Unit: fixed point value q30 of cosine of the angle Range: [130856211 - 1069655912], corresponding to angle between 5 and 85 degrees Default: 1046221864, corresponding to an angle of 13 degrees
IMEM_SRAM	IMEM_SRAM_REG_561 R2W_MOTION_THR_ANGLE_COSINE[15:8]	0x231	1	
	IMEM_SRAM_REG_562 R2W_MOTION_THR_ANGLE_COSINE[23:16]	0x232	1	
	IMEM_SRAM_REG_563 R2W_MOTION_THR_ANGLE_COSINE[31:24]	0x233	1	
	IMEM_SRAM_REG_564 R2W_MOTION_THR_TIMER_FAST[7:0]	0x234	1	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is Y axis up (with less than 30 degrees of inclination). Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 500] Default: 240
	IMEM_SRAM_REG_565 R2W_MOTION_THR_TIMER_FAST[15:8]	0x235	1	
	IMEM_SRAM_REG_566 R2W_MOTION_THR_TIMER_FAST[23:16]	0x236	1	
	IMEM_SRAM_REG_567 R2W_MOTION_THR_TIMER_FAST[31:24]	0x237	1	
	IMEM_SRAM_REG_568 R2W_MOTION_THR_TIMER_SLOW[7:0]	0x238	1	Timer relative to the rapidity of the algorithm to trigger wake up when the orientation before motion is over 30 degrees on the Y axis
	IMEM_SRAM_REG_569 R2W_MOTION_THR_TIMER_SLOW[15:8]	0x239	1	

	IMEM_SRAM_REG_570 R2W_MOTION_THR_TIMER_SLOW[23:16]	0x23A	1	Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [240- 1000] Default: 500
	IMEM_SRAM_REG_571 R2W_MOTION_THR_TIMER_SLOW[31:24]	0x23B	1	
	IMEM_SRAM_REG_572 R2W_MOTION_PREV_GRAVITY_TIMEOUT[7:0]	0x23C	1	Time delay to update internal value of previous gravity when no motion is detected. Longer time enables detection motion during slower gesture. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 300
	IMEM_SRAM_REG_573 R2W_MOTION_PREV_GRAVITY_TIMEOUT[15:8]	0x23D	1	
	IMEM_SRAM_REG_574 R2W_MOTION_PREV_GRAVITY_TIMEOUT[23:16]	0x23E	1	
	IMEM_SRAM_REG_575 R2W_MOTION_PREV_GRAVITY_TIMEOUT[31:24]	0x23F	1	
	IMEM_SRAM_REG_576 R2W_LAST_GRAVITY_MOTION_TIMER[7:0]	0x240	1	Time delay to update the current gravity estimator when no motion is detected. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 480
	IMEM_SRAM_REG_577 R2W_LAST_GRAVITY_MOTION_TIMER[15:8]	0x241	1	
	IMEM_SRAM_REG_578 R2W_LAST_GRAVITY_MOTION_TIMER[23:16]	0x242	1	
	IMEM_SRAM_REG_579 R2W_LAST_GRAVITY_MOTION_TIMER[31:24]	0x243	1	
	IMEM_SRAM_REG_580 R2W_LAST_GRAVITY_TIMEOUT[7:0]	0x244	1	Time delay to update gravity in case motion is detected all the time, force to update gravity estimator even if the device is not stable. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [1000 - 10000] Default: 2600
	IMEM_SRAM_REG_581 R2W_LAST_GRAVITY_TIMEOUT[15:8]	0x245	1	
	IMEM_SRAM_REG_582 R2W_LAST_GRAVITY_TIMEOUT[23:16]	0x246	1	
	IMEM_SRAM_REG_583 R2W_LAST_GRAVITY_TIMEOUT[31:24]	0x247	1	
	IMEM_SRAM_REG_584 R2W_GESTURE_VALIDITY_TIMEOUT[7:0]	0x248	1	If gesture is not completed in this timeout limit, gesture is invalid. Unit: ms (no dependency on ODR, it is managed internally by the algorithm) Range: [100 - 1000] Default: 240
	IMEM_SRAM_REG_585 R2W_GESTURE_VALIDITY_TIMEOUT[15:8]	0x249	1	
	IMEM_SRAM_REG_586 R2W_GESTURE_VALIDITY_TIMEOUT[23:16]	0x24A	1	
	IMEM_SRAM_REG_587 R2W_GESTURE_VALIDITY_TIMEOUT[31:24]	0x24B	1	

4.2.3.6 LowG/HighG/Freefall parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_316 LOWG_PEAK_TH[7:0]	0x13C	1	Threshold for accel values below which low-g state is detected. Unit: g in q12 Range: [128 - 4096] Default: 2048
	IMEM_SRAM_REG_317 LOWG_PEAK_TH[15:8]	0x13D	1	
	IMEM_SRAM_REG_318 LOWG_PEAK_TH_HYST[7:0]	0x13E	1	Hysteresis value added to the low-g threshold after exceeding it. Unit: g in q12 Range: [128 – 1024] Default: 128
	IMEM_SRAM_REG_319 LOWG_PEAK_TH_HYST[15:8]	0x13F	1	
	IMEM_SRAM_REG_320 LOWG_TIME_TH[7:0]	0x140	1	Number of samples required to enter low-g state. Unit: time in samples number Range: [1 – 300] Default: 13 (set for default ODR = 800 Hz, equivalent to 16 ms)
	IMEM_SRAM_REG_321 LOWG_TIME_TH[15:8]	0x141	1	
	IMEM_SRAM_REG_304 HIGHG_PEAK_TH[7:0]	0x130	1	Threshold for accel values above which high-g state is detected. Unit: g in q12 Range: [1024 – 32768] Default: 29696
	IMEM_SRAM_REG_305 HIGHG_PEAK_TH[15:8]	0x131	1	
	IMEM_SRAM_REG_306 HIGHG_PEAK_TH_HYST[7:0]	0x132	1	Hysteresis value subtracted from the high-g threshold after exceeding it. Unit: g in q12 Range: [128 – 1024] Default: 640
	IMEM_SRAM_REG_307 HIGHG_PEAK_TH_HYST[15:8]	0x133	1	
	IMEM_SRAM_REG_308 HIGHG_TIME_TH[7:0]	0x134	1	Threshold for accel values above which high-g state is detected. Unit: time in samples number Range: [1-300] Default: 1 (set for default ODR = 800 Hz, equivalent to 1.25 ms)
	IMEM_SRAM_REG_309 HIGHG_TIME_TH[15:8]	0x135	1	
	IMEM_SRAM_REG_288 FF_MIN_DURATION[7:0]	0x120	1	Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 – 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms)
	IMEM_SRAM_REG_289 FF_MIN_DURATION[15:8]	0x121	1	
	IMEM_SRAM_REG_290 FF_MIN_DURATION[23:16]	0x122	1	
	IMEM_SRAM_REG_291 FF_MIN_DURATION[31:24]	0x123	1	
	IMEM_SRAM_REG_292 FF_MAX_DURATION[7:0]	0x124	1	Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 – 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms)
	IMEM_SRAM_REG_293 FF_MAX_DURATION[15:8]	0x125	1	
	IMEM_SRAM_REG_294 FF_MAX_DURATION[23:16]	0x126	1	
	IMEM_SRAM_REG_295 FF_MAX_DURATION[31:24]	0x127	1	
	IMEM_SRAM_REG_296 FF_DEBOUNCE_DURATION[7:0]	0x128	1	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 – 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1s)
	IMEM_SRAM_REG_297 FF_DEBOUNCE_DURATION[15:8]	0x129	1	
	IMEM_SRAM_REG_298 FF_DEBOUNCE_DURATION[23:16]	0x12A	1	
	IMEM_SRAM_REG_299 FF_DEBOUNCE_DURATION[31:24]	0x12B	1	

4.2.3.7 TAP parameters

Reg. Bank (base addr.)	Register/Field Name	Addr	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_403 TAP_MIN_JERK	0x193	1	The minimal value of jerk to be considered as a tap candidate. Unit: g in q6 Range: [0 - 64] Default: 17
	IMEM_SRAM_REG_400 TAP_TMAX[7:0]	0x190	1	size of the analysis window to detect tap events (single-tap or double-tap) unit: time in sample number range: [49 – 496] default: 99 (set for default ODR = 200Hz, equivalent to. 0.5s)
	IMEM_SRAM_REG_401 TAP_TMAX[15:8]	0x191	1	
	IMEM_SRAM_REG_402 TAP_TMIN	0x192	1	Single tap window, sub-windows within Tmax to detect single-tap event. Unit: time in sample number Range: [24 – 184] Default: 33 (set for default ODR = 200Hz, equivalent to. 0.165 s)
	IMEM_SRAM_REG_405 TAP_MAX_PEAK_TOL	0x195	1	Maximum peak tolerance is the percentage of pulse amplitude to get the smudge threshold for rejection. Unit: N/A Range: [1 (12.5%) 2 (25.0%) 3 (37.5%) 4 (50.0 %)] Default: 2
	IMEM_SRAM_REG_404 TAP_SMUDGE_REJECT_THR	0x194	1	Max acceptable number of samples (jerk value) over tap_max_peak_tol the during the Tmin window. Over this value, Tap event is rejected unit: time in number of samples range: [13 – 92] Default: 17 (set for default ODR = 200Hz, equivalent to 0.085s)
	IMEM_SRAM_REG_406 TAP_TAVG	0x196	1	Energy measurement window size to determine the tap axis associated with the 1st tap. Unit: time in sample number Range: [1 ; 2 ; 4 ; 8] Default: 8

4.2.4 Output registers and data

Reg. Bank	Register/Field Name	Addr	Bit Field	Functionality
USER BANK 0	INT_APEX_STATUS0	0x3B	INT_STATUS_TAP_DETECT	1: Tap detection interrupt occurred. 0: Tap detection interrupt did not occur.
			INT_STATUS_HIGH_G_DET	1: highG detection interrupt occurred. 0: highG detection interrupt did not occur.
			INT_STATUS_LOW_G_DET	1: lowG detection interrupt occurred. 0: lowG detection interrupt did not occur.
			INT_STATUS_TILT_DET	1: tilt detection interrupt occurred. 0: tilt detection interrupt did not occur.
			INT_STATUS_STEP_CNT_OVFL	1: stepcount overflow interrupt occurred. 0: stepcount overflow interrupt did not occur.
			INT_STATUS_STEP_DET	1: step detection interrupt occurred. 0: step detection interrupt did not occur.
			INT_STATUS_FF_DET	1: freefall interrupt occurred. 0: freefall interrupt did not occur.
			INT_STATUS_R2W_WAKE_DET	1: wake interrupt occurred. 0: wake interrupt did not occur.
	INT_APEX_STATUS1	0x3C	INT_STATUS_R2W_SLEEP_DET	1: sleep interrupt occurred. 0: sleep interrupt did not occur.
			INT_STATUS_SMD_DET	1: SMD interrupt occurred. 0: SMD interrupt did not occur.

Reg. Bank	Register/Field Name	Addr.	Size (Bytes)	Functionality
IMEM_SRAM	IMEM_SRAM_REG_141 TAP_NUM	0x8D	1	Type of the last reported TAP event: 0: no tap, 1: single tap, 2: double tap
	IMEM_SRAM_REG_142 TAP_AXIS	0x8E	1	Indicate the axis of the tap in the device frame. 0: ax, 1: ay, 2: az
	IMEM_SRAM_REG_143 TAP_DIR	0x8F	1	Indicate the direction of the tap in the device frame. 0: positive, 1: negative
	IMEM_SRAM_REG_154 PED_STEP_CNT_BUF1[7:0]	0x9A	1	Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF2. Unit: number of steps
	IMEM_SRAM_REG_155 PED_STEP_CNT_BUF1[15:8]	0x9B	1	
	IMEM_SRAM_REG_156 PED_STEP_CNT_BUF2[7:0]	0x9C	1	Number of steps done since the last init of the pedometer feature. Filled in alternatively with PED_STEP_CNT_BUF1. Unit: number of steps.
	IMEM_SRAM_REG_157 PED_STEP_CNT_BUF2[15:8]	0c9D	1	
	IMEM_SRAM_REG_159 PED_STEP_CADENCE	0c9F	1	Instant step cadence measured by the algorithm Unit: 4*number of samples between two consecutive steps. Cadency (step/s) = (ped_step_cadence / 4) / (pedometer_ ODR).
	IMEM_SRAM_REG_160 POWER_ACTIVITY_CLASS	0xA0	1	Activity classification of step detected. 00000000: Unknown 00000001: Walk 00000010: Run Others: Reserved
	IMEM_SRAM_REG_144 DOUBLE_TAP_TIMING	0x90	1	In case of double tap, indicate the sample count between the two detected pulses. Double tap timing in seconds is double_tap_timing / ACCEL_ODR_Hz

	IMEM_SRAM_REG_136 FF_DURATION_BUF1[7:0]	0x88	1	number of samples. Freefall duration in seconds is ff_duration_buf1 / ACCEL_ODR_Hz
	IMEM_SRAM_REG_137 FF_DURATION_BUF1[15:8]	0x89	1	
	IMEM_SRAM_REG_138 FF_DURATION_BUF2[7:0]	0x8A	1	number of samples. Freefall duration in seconds is ff_duration_buf2 / ACCEL_ODR_Hz
	IMEM_SRAM_REG_138 FF_DURATION_BUF2[15:8]	0x8B	1	

4.3 CONFIGURE AND RUN APEX FEATURES

Running APEX feature requires host software to execute the following sequence of actions:

Step 1: Configure accelerometer
Step 2: Configure eDMP
Step 3: Configure APEX parameters
Step 4: Enable relevant APEX interrupts
Step 5: Enable accelerometer and eDMP

Next chapters detail each item.

4.3.1 Step 1: Configure accelerometer

4.3.1.1 Note on ODR

Both Accel and eDMP ODR should be set by the host. The accel_odr should be faster than or equal to the apex_odr. Hardware automatically decimates the signal path output so samples seen by eDMP will always be at apex_odr.

Accel low power mode (LP) is only supported for ODR <= 400 Hz. For ODR > 400 Hz, operation mode should be low noise (LN). The host is responsible for setting valid operation mode for selected DMP-ODR.

eDMP automatically selects APEX algorithms ODR according to apex_odr when running eDMP initialization procedure as shown in the following table:

edmp_odr	pedometer	SMD	Tilt	r2w	Freefall	HighG	LowG	Tap
800	50	50	50	100	800	800	800	800
400	50	50	50	100	400	400	400	400
200	50	50	50	100	200	200	200	200
100	50	50	50	100	100	100	100	N/A
50	50	50	50	50	50	50	50	N/A
25	25	N/A	25	25	25	25	25	N/A

4.3.1.2 Accel configuration sequence

Field Name	Register Name	Register Address (bit)	Bank	Description
ACCEL_ODR	ACCEL_CONFIG0	0x1B(3:0)	Bank 0	Set Accel ODR
ACCEL_UI_LPFBW_SEL	IPREG_SYS2_REG_131	0x83(2:0)	IPREG_SYS2	Set Accel Low noise bandwidth
ACCEL_LP_AVG_SEL	IPREG_SYS2_REG_129	0x81(3:0)	IPREG_SYS2	Set Accel low Power averaging
ACCEL_LP_CLK_SEL	SMC_CONTROL_0	0x58(4)	IPREG_TOP1	Set Accel low power clock source

4.3.2 Step 2: Configure eDMP

Field Name	Register Name	Register Address (bit)	Bank	Description
APEX_ODR	DMP_EXT_SEN_ODR_CFG	0x27 (2:0)	Bank 0	Set DMP ODR
EDMP_APEX_EN0	EDMP_APEX_EN0	0x29		Set all bits 0 so all DMP features are disabled before init.
EDMP_APEX_EN0	EDMP_APEX_EN1	0x2A		Set all bits 0 so all DMP features are disabled before init.
PRGM_STRT_ADDR_IRQ_0[7:0]	EDMP_PRGRM_IRQ0_0	0x4F(7:0)	IPREG_TOP1	LSB for Program Address 0 value 0x00
PRGM_STRT_ADDR_IRQ_0[15:8]	EDMP_PRGRM_IRQ0_1	0x50(7:0)		MSB for Program Address 0 value 0x40
PRGM_STRT_ADDR_IRQ_1[7:0]	EDMP_PRGRM_IRQ1_0	0x51(7:0)		LSB for Program Address 1 value 0x04
PRGM_STRT_ADDR_IRQ_1[15:8]	EDMP_PRGRM_IRQ1_1	0x52(7:0)		MSB for Program Address 1 value 0x40
PRGM_STRT_ADDR_IRQ_2[7:0]	EDMP_PRGRM_IRQ2_0	0x53(7:0)		LSB for Program Address 2 value 0x08
PRGM_STRT_ADDR_IRQ_2[15:8]	EDMP_PRGRM_IRQ2_1	0x54(7:0)		MSB for Program Address 2 value 0x40
EDMP_SP_START_ADDR	EDMP_SP_START_ADDR	0x55(7:0)		EDMP Start address value 0x05
STEP_COUNT_HOST_RPTR	APEX_BUFFER_MGMT	0x2B(3:2)	Bank 0	Initialize read pointer for pedometer value 0x02
STEP_COUNT_EDMP_WPTR	APEX_BUFFER_MGMT	0x2B(1:0)		Initialize write pointer for pedometer value 0x00
FF_DURATION_HOST_RPTR	APEX_BUFFER_MGMT	0x2B(7:6)		Initialize read pointer for pedometer value 0x00
FF_DURATION_EDMP_WPTR	APEX_BUFFER_MGMT	0x2B(5:4)		Initialize write pointer for pedometer value 0x00
FIFO_GSLEEP_SHARED_SRAM	FIFO_SRAM_SLEEP	0xA7(1:0)	IPREG_TOP1	Power Up eDMP SRAM value 0x03
Clear SRAM by doing indirect write at location 0x0000 to 0x04BF using register IREG_ADDR7_0, IREF_ADDR_15_8 and IREG Data. Refer datasheet section Indirect register Access.				
INTI_EN	EDMP_APEX_EN1	0x2A(1)	Bank 0	Set bit to 1 to Init EDMP procedure.
INT_ON_DEMAND_PIN_0_DIS	STATUS_MASK_PIN_0_7	0x71(5)	IPREG_TOP1	Clear eDMP on-demand interrupt source mask by setting 0
EDMP_EN	EDMP_APEX_EN1	0x2A(6)	Bank 0	Set bit to 1 to enable EDMP.
EDMP_ON_DEMAND_EN	REG_HOST_MSG	0x73(5)		Set to 1 to trigger on demand.
wait 200 usec				
EDMP_IDLE	IPREG_MISC	0x97(1)	IPREG_TOP1	Loop till value read is 1
INT_ON_DEMAND_PIN_0_DIS	STATUS_MASK_PIN_0_7	0x71(5)		Set eDMP on-demand interrupt source mask by setting 1
EDMP_EN	EDMP_APEX_EN1	0x2A(6)	Bank 0	Set bit to 0 to disable eDMP.
INT_ACCEL_DRDY_PIN_0_DIS	STATUS_MASK_PIN_0_7	0x71(0)	IPREG_TOP1	Set bit 0.

4.3.3 Step 3: Configure APEX parameters

At this step, eDMP initialization procedure sets some default values for every APEX parameter. User might want to change some (or all) of them. The list of parameters for each algorithm is given in the previous chapter.

4.3.3.1 Algorithm dependencies

There are a few dependencies between APEX features that need to be considered when configuring parameters.

SMD reuses some internal processing from pedometer. eDMP automatically runs pedometer when SMD is enabled. When configuring SMD, the user should make sure pedometer and SMD parameters are correctly configured.

Freefall uses LowG and HighG. When configuring Freefall, the user should make sure LowG, highG, and Freefall parameters are correctly configured.

4.3.3.2 APEX power saving

ICM-45605 and ICM-45686 embeds a power saving mechanism for APEX. This disables APEX execution when no motion is detected after a programmable time.

The user can enable Power Save Mode (POWER_SAVE_EN = 1 and POWER_SAVE_TIME > 0) with WOM (WOM_EN=1). Power Save Mode uses the WOM thresholds (ACCEL_WOM_X/Y/Z_THR) to enable/disable the other APEX routines during stationary periods, thus reducing the processing load on the chip.

In addition to APEX parameters, the user can choose to enable power saving by following this sequence:

Field Name	Register Name	Register Address (bit)	Bank	Description
POWER_SAVE_TIME [7:0]	IMEM_SRAM_REG_196	0xC4 (7:0)	IMEM_SRAM	Set power save time threshold
POWER_SAVE_TIME [15:8)	IMEM_SRAM_REG_197	0xC5 (7:0)		Set power save time threshold
POWER_SAVE_TIME [23:16]	IMEM_SRAM_REG_198	0xC6 (7:0)		Set power save time threshold
POWER_SAVE_TIME [31:24)	IMEM_SRAM_REG_199	0xC7 (7:0)		Set power save time threshold
ACCEL_WOM_X_THR	ACCEL_WOM_X_THR	0x7E (7:0)	IPREG_TOP1	Set X-axis WOM threshold
ACCEL_WOM_Y_THR	ACCEL_WOM_Y_THR	0x7F (7:0)		Set Y-axis WOM threshold
ACCEL_WOM_Z_THR	ACCEL_WOM_Z_THR	0x80 (7:0)		Set Z-axis WOM threshold
WOM_EN	TMST_WOM_CONFIG	0x23(4)	Bank 0	WOM enable
WOM_MODE		0x23(3)		WOM mode select
POWER_SAVE_EN	EDMP_APEX_EN1	0x2A(2)		Power save enable

4.3.4 Step 4: Enable relevant APEX interrupts

Field Name	Register Name	Register Address (bit)	Bank	Description
INT_STATUS_MASK_PIN_TAP_DETECT	INT_APEX_CONFIG0	0x39 (0)	Bank 0	Set 1 to mask tap interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_HIGH_G_DET		0x39 (1)		Set 1 to mask high g interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_LOW_G_DET		0x39 (2)		Set 1 to mask low g interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_TILT_DET		0x39 (3)		Set 1 to mask tilt interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_STEP_CNT_OVFL		0x39 (4)		Set 1 to mask step overflow interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_STEP_DET		0x39 (5)		Set 1 to mask step detect interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_FF_DET		0x39 (6)		Set 1 to mask freefall interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_R2W_WAKE_DET		0x39 (7)		Set 1 to mask r2w wake interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_R2W_SLEEP_DET	INT_APEX_CONFIG1	0x3A (0)		Set 1 to mask r2w sleep interrupt and 0 to unmask.
INT_STATUS_MASK_PIN_SMD_DET		0x3A (1)		Set 1 to mask smd detect interrupt and 0 to unmask.
INT1_STATUS_EN_APEX_EVENT	INT1_CONFIG1	0x17 (6)		Enable apex event interrupts on Int1
INT2_STATUS_EN_APEX_EVENT	INT2_CONFIG1	0x57 (6)		Enable apex event interrupts on Int2

4.3.5 Step 5: Enable accelerometer and APEX features

4.3.5.1 Note on LowG, HighG features control

HighG and LowG have no specific enable bits. These features are controlled with the EDMP_APEX_EN0.ff_en bit, meaning enabling Freefall enables Freefall, HighG, and LowG algorithms.

The user should unmask relevant output interrupts in INT_APEX_CONFIGX registers to receive targeted events only.

4.3.5.2 Register access sequence

Field Name	Register Name	Register Address (bit)	Bank	Description
ACCEL_MODE	PWR_MGMT0	0x10 (1:0)	Bank 0	3 if ODR >= 800 else 2
TAP_EN	EDMP_APEX_EN0	0x29 (0)		Set 1 to enable tap.
TILT_EN		0x29 (3)		Set 1 to enable tilt.
PEDO_EN		0x29 (4)		Set 1 to enable pedometer.
FF_EN		0x29 (5)		Set 1 to enable freefall.
R2W_EN		0x29 (6)		Set 1 to enable raise 2wake.
SMD_EN		0x29 (7)		Set 1 to enable smd.
EDMP_EN	EDMP_APEX_EN1	0x2A(6)		Set to 1 to enable EDMP

4.4 APEX OUTPUT

4.4.1 APEX output events

APEX events are signaled in a set of two registers, namely INT_APEX_STATUS0 and INT_APEX_STATUS1.

Note: to safely handle interrupt deassertion, these two registers should be read in one single burst transaction.

4.4.2 APEX output data

In addition to APEX events, some APEX features report more information, namely:

pedometer step count
pedometer cadence
pedometer activity class
freefall duration
tap type
tap axis
tap direction
double tap timing

These APEX outputs are in internal SRAM (IMEM_SRAM bank) and are documented in the previous chapter.

4.4.2.1 Reading pedometer step count

Pedometer step_count is a 2-byte field that is shared between eDMP and the host. To avoid any concurrent access issue between the host and eDMP, step count value should be read multiple times until the same value is read twice consecutively.

4.4.2.2 Reading freefall duration

Freefall duration is a 2-byte field that is shared between eDMP and the host. To avoid any concurrent access issue between the host and eDMP, a 2-entry buffer is used to make sure the host never reads the same buffer entry than Freefall is writing to. The following sequence should be strictly implemented to read coherent data:

```
# Read ff_duration
status |= inv_imu_read_reg(s, APEX_BUFFER_MGMT, 1, (uint8_t *)&apex_buffer_mgmt);
edmp_wptr = APEX_BUFFER_MGMT.ff_duration_edmp_wptr
host_rptr = APEX_BUFFER_MGMT.ff_duration_host_rptr
if (host_rprt != edmp_wptr)
    if ((host_rptr & 0x1) == 0)
        freefall_duration = IMEM_SRAM.ff_duration_buf1
    else
        freefall_duration = IMEM_SRAM.ff_duration_buf2
host_rptr = (host_rptr + 1) & 0x3
apex_buffer_mgmt.ff_duration_host_rptr = host_rptr;
status |= inv_imu_write_reg(s, APEX_BUFFER_MGMT, 1, (uint8_t *)&apex_buffer_mgmt);

#define APEX_BUFFER_MGMT                    0x2b
typedef struct {
    uint8_t ff_duration_host_rptr           : 2;
    uint8_t ff_duration_edmp_wptr           : 2;
    uint8_t step_count_host_rptr            : 2;
    uint8_t step_count_edmp_wptr            : 2;
} apex_buffer_mgmt_t;
```

4.5 WAKE ON MOTION (WOM)

Wake on Motion detects when the change in accelerometer output exceeds a user-programmable threshold. WOM can assert an interrupt if the accelerometer 1st order difference is greater than a threshold or if the accelerometer change (relative to the first sample after WOM is enabled) is greater than a threshold.
The user can program independent acceleration thresholds for all 3 axes and configure the part to assert an interrupt when ANY axis trips its threshold, or when ALL axes trip their thresholds simultaneously.

4.5.1 Configuration registers

Field Name	Register Name	Register Address (bit)	Bank	Description
ACCEL_WOM_X_THR	ACCEL_WOM_X_THR	0x7E	IPREG_TOP1	Set X-axis WOM threshold
ACCEL_WOM_Y_THR	ACCEL_WOM_Y_THR	0x7F		Set Y-axis WOM threshold
ACCEL_WOM_Z_THR	ACCEL_WOM_Z_THR	0x80		Set Z-axis WOM threshold
WOM_EN	TMST_WOM_CONFIG	0x23(4)	Bank 0	WOM enable
WOM_MODE		0x23(3)		WOM mode select
WOM_INT_MODE		0x23(2)		WOM interrupt mode
WOM_INT_DURATION		0x23(1:0)		0: WOM interrupt asserted at first over threshold event 1: WOM interrupt asserted at second over threshold event 2: WOM interrupt asserted at third over threshold event 3: WOM interrupt asserted at fourth over threshold event

4.5.2 WOM initialization procedure

This example case is WOM for 200mg X/Y/Z or condition, compared with previous sample

Field Name	Register Name	Register Address (bit)	Bank	Value	Description
ACCEL_WOM_X_THR	ACCEL_WOM_X_THR	0x7E	IPREG_TOP1	0x32	Set X-axis WOM threshold, example 200mg
ACCEL_WOM_Y_THR	ACCEL_WOM_Y_THR	0x7F		0x32	Set Y-axis WOM threshold example 200mg
ACCEL_WOM_Z_THR	ACCEL_WOM_Z_THR	0x80		0x32	Set Z-axis WOM threshold example 200mg
WOM_EN	TMST_WOM_CONFIG	0x23(4)	Bank 0	1	WOM enable
WOM_MODE		0x23(3)		1	WOM mode select 0: Compared with initial sample 1: Compared with previous sample
WOM_INT_MODE		0x23(2)		0	0: WOM from 3 axes are ORed 1: WOM from 3 axes are ANDed
WOM_INT_DURATION		0x23(1:0)		0	0: WOM interrupt asserted at first over threshold event 1: WOM interrupt asserted at second over threshold event 2: WOM interrupt asserted at third over threshold event 3: WOM interrupt asserted at fourth over threshold event
int1_status_en_wom_x	INT1_CONFIG1	0x17(1)		1	Enable WOM X interrupt
int1_status_en_wom_y		0x17(2)		1	Enable WOM Y interrupt
int1_status_en_wom_z		0x17(3)		1	Enable WOM Z interrupt

4.5.3 WOM output interrupt

Field Name	Register Name	Register Address (bit)	Bank	Description
int1_status_wom_x	INT1_STATUS1	0x1A(1)	Bank 0	1: WOM Z interrupt occurred.
int1_status_wom_y		0x1A(2)		1: WOM Y interrupt occurred.
int1_status_wom_z		0x1A(3)		1: WOM Z interrupt occurred.

5 OPERATION POWER MODES

Multiple power modes are designed to meet different power consumption requirements in application.

The accel and gyro sensors in ICM-45605 and ICM-45686 can be operated in OFF, STBY (gyro), LP, ULP (accel), and LN modes based on the setting of the appropriate power management registers.

STBY = Gyro Standby
GLN = Gyro Low Noise Mode
ALN = Accel Low Noise Mode
CLN = Combination Low Noise Mode (GLN + ALN)
GLP = Gyro Low Power Mode
ALP = Accel Low power Mode
AULP = Accel Ultra-low Power Mode
CLP = Combination Low Power Mode (GLP + ALP)

ICM-45686 has two digital communication interfaces, AP/AUX1, work independently. Table 1 lists the combination of supported modes between them.

When gyro and/or accel are enabled through AUX1 interface, the related sensor operates in LN only.

AP		AUX1
G=OFF	A=LN	CLN or GLN
	A=LP	
	A=ULP	
G=STBY	A=LN	CLN, GLN or ALN
	A=LP	
	A=ULP	
G=LP	A=LN	CLN, GLN or ALN
	A=LP	
	A=ULP	
G=LN	A=LN	CLN, GLN or ALN
	A=LP	
	A=ULP	

Table 1. Operation mode for two interfaces

5.1 ICM-45605 AND ICM-45686 SLEEP MODE

To achieve low power consumption in sleep mode, there is a limited number of function blocks that have the supply to guarantee a minimum set of functionalities, such as serial interface operations for AP/AUX1 or storage of register map configurations written by the user or loaded from OTP after a power-on reset.

When the ICM-45605 and ICM-45686 chip is in sleep mode, the chip does not support the reading of sensor data registers from any host (AP, AUX1). There will be no sensor-data-ready (DRDY) interrupt generated.

Before turning off all sensors to transition the ICM-45605 and ICM-45686 into the sleep mode, the host (AP, AUX1) should complete its sensor data register read operation.

To bring the ICM-45605 and ICM-45686 into sleep mode, the registers below need to be set. The power consumption of the sleep mode is documented in the datasheet.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
3:2	GYRO_MODE	00: Turns gyroscope off
1:0	ACCEL_MODE	00: Turns accelerometer off

Name: PWR_MGMT_AUX1
Bank: User bank 0
Address: 0x54

BIT	NAME	FUNCTION
1	GYRO_AUX1_EN	0: OFF
0	ACCEL_AUX1_EN	0: OFF

5.2 GYRO OPERATION MODES

ICM-45605 and ICM-45686 gyro operation mode can be set through AP/AUX1 independently.

When gyro is enabled in AUX1, only low noise mode is supported.

Through AP interface, three different gyro operation modes can be selected.

STBY
GLN
GLP

Each operation mode will be explained in detail.

5.2.1 Gyro off mode

To disable the ICM-45605 and ICM-45686 gyro, all the AP and AUX1 must turn the gyro off.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
3:2	GYRO_MODE	00: Turns gyroscope off

Name: PWR_MGMT_AUX1
Bank: User bank 0
Address: 0x54

BIT	NAME	FUNCTION
1	GYRO_AUX1_EN	0: OFF

5.2.2 Gyro low noise mode

The gyro low noise mode can be enabled through AP and AUX1 interfaces independently. Any one of the settings below will bring the gyro into low noise mode. The power consumption and gyro noise level in this mode are specified in the datasheet. This is the best gyro performance mode.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
3:2	GYRO_MODE	11: Places gyroscope in Low Noise (LN) Mode

Name: PWR_MGMT_AUX1
Bank: User bank 0
Address: 0x54

BIT	NAME	FUNCTION
1	GYRO_AUX1_EN	1: ON

5.2.3 Gyro standby mode

To quick start gyro, ICM-45605 and ICM-45686 has a gyro standby mode that can be set through AP interface only. In this mode, gyro drive remains on, but sense is off for power saving.

To bring gyro into standby mode, the registers below need to be set.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
3:2	GYRO_MODE	01: Places gyroscope in Standby Mode

Name: PWR_MGMT_AUX1
Bank: User bank 0
Address: 0x54

BIT	NAME	FUNCTION
1	GYRO_AUX1_EN	0: OFF

5.2.4 Gyro low power mode

To achieve low power consumption, ICM-45605 and ICM-45686 can put gyro into duty-cycled operation. Multiple sample average selections allow the user to optimize gyro noise and power consumption in applications.

The gyro low power mode can be set through AP interface only. To bring gyro into low power mode, the registers below need to be set.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
3:2	GYRO_MODE	10: Places gyroscope in Low Power (LP) Mode

Name: PWR_MGMT_AUX1 Bank: User bank 0 Address: 0x54		
BIT	**NAME**	**FUNCTION**
1	GYRO_AUX1_EN	0: OFF

Gyro ODR in low power mode is set through this register. The GLP highest ODR is 400 Hz.

Name: GYRO_CONFIG0 Bank: User bank 0 Address: 0x1C		
BIT	**NAME**	**FUNCTION**
3:0	GYRO_ODR	Gyroscope ODR selection for UI interface output 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode)

The sample data averaging selection is set through GYRO_LP_AVG_SEL.

Name: IPREG_SYS1_REG_170 Bank: IPREG_SYS1 Address: 0xAA		
BIT	**NAME**	**FUNCTION**
4:1	GYRO_LP_AVG_SEL	Gyro Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved

The power consumption, Ton time, and noise level depend on data sample average number and output data rate (ODR).

5.3 ACCEL OPERATION MODES

ICM-45605 and ICM-45686 accel operation mode can be set through AP/AUX1 independently. When accel is enabled in AUX1, only low noise mode is supported.

AP interface supports three different accel operation modes.

ALN
ALP
AULP

When the SREG_AUX_ACCEL_ONLY_EN = 0 (manufacture default value), the AUX1 supports CLN and GLN.

When the SREG_AUX_ACCEL_ONLY_EN = 1 (through user set), the AUX1 supports CLN, GLN, and ALN.

Name: SMC_CONTROL_1
Bank: IPREG_TOP1
Address: 0x59

BIT	NAME	FUNCTION
3	SREG_AUX_ACCEL_ONLY_EN	0: Sensor data register read from AUX1 interfaces is supported only if gyro sensor is enabled. 1: Sensor data register read from AUX1 interfaces is supported even if gyro sensor is not enabled.

Each operation mode will be explained in detail.

5.3.1 Accel off mode

To disable the ICM-45605 and ICM-45686 accel, AP and AUX1 must all turn the accel off.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
1:0	ACCEL_MODE	00: Turns accelerometer off 01: Turns accelerometer off

Name: PWR_MGMT_AUX1
Bank: User bank 0
Address: 0x54

BIT	NAME	FUNCTION
0	ACCEL_AUX1_EN	0: OFF

5.3.2 Accel low noise mode

When SREG_AUX_ACCEL_ONLY_EN = 1, the accel low noise mode can be enabled through AP and AUX1 interfaces independently.

Any one of the settings below will bring the accel into low noise mode. The power consumption and noise level in this mode are specified in the datasheet. This is the best accel performance mode.

Name: PWR_MGMT0
Bank: User bank 0
Address: 0x10

BIT	NAME	FUNCTION
1:0	ACCEL_MODE	11: Places accelerometer in Low Noise (LN) Mode

Name: PWR_MGMT_AUX1 Bank: User bank 0 Address: 0x54		
BIT	**NAME**	**FUNCTION**
0	ACCEL_AUX1_EN	1: ON

5.3.3 Accel Low Power (ALP) and Ultra-Low Power Mode (AULP)

To achieve low power consumption, ICM-45605 and ICM-45686 supports accel duty-cycled operation. Multiple sample average selections allow the user to optimize accel noise, bandwidth, and power consumption in applications.

ICM-45605 and ICM-45686 has two low power modes, ALP, and AULP. Their settings and performance will be discussed in this section.

The power consumption, noise level, and bandwidth depend on data sample average number and data out rate (ODR).

5.3.3.1 Configurations

Configuring the following register fields will bring accel to ALP or AULP mode.

Name: PWR_MGMT0 Bank: User bank 0 Address: 0x10		
BIT	**NAME**	**FUNCTION**
1:0	ACCEL_MODE	10: Places accelerometer in Low Power (LP) Mode

Name: PWR_MGMT_AUX1 Bank: User bank 0 Address: 0x54		
BIT	**NAME**	**FUNCTION**
0	ACCEL_AUX1_EN	0: OFF

ALP or AULP is set through ACCEL_LP_CLK_SEL.

Name: SMC_CONTROL_0 Bank: IPREG_TOP1 Address: 0x58		
BIT	**NAME**	**FUNCTION**
4	ACCEL_LP_CLK_SEL	This bit is applicable to host interface operation. A. When RTC mode is not enabled (or RTC_MODE = 0): This bit is effective when the host interface is in accel only operation with ACCEL_MODE set to LP mode. 0: Host interface is in AULP mode. 1: Host interface is in ALP mode. When I3C^{SM} Synchronous Timing Control function is enabled on host interface, if the host interface is in accel only operation with ACCEL_MODE set to LP mode, ACCEL_LP_CLK_SEL must be set to 1. I3C^{SM} Synchronous

		Timing Control may not generate correct timing if ACCEL_LP_CLK_SEL is set to 0. B. When RTC mode is enabled (or RTC_MODE = 1): Independent of enabling/disabling of I3C^{SM} Synchronous timing control function, ACCEL_LP_CLK_SEL must be set to 1. Dynamic Change Supported.

Accel ODR in low power mode is set through this register. The highest ODR supported in the ALP/AULP mode is 400 Hz.

Name: ACCEL_CONFIG0
Bank: User bank 0
Address: 0x1B

BIT	NAME	FUNCTION
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode)

The sample data averaging selection is set through ACCEL_LP_AVG_SEL.

Name: IPREG_SYS2_REG_129
Bank: IPREG_SYS2
Address: 0x81

BIT	NAME	FUNCTION
3:0	ACCEL_LP_AVG_SEL	Accel Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved

5.3.3.2 Operation limitation for Accel ULP

To maintain ultra-low power for AULP mode, some function blocks are disabled. The non-supported functions in AULP mode are listed below.

The ICM-45605 and ICM-45686 does not support the reading of sensor data registers from any host (AP and AUX1). AP host needs to retrieve sensor data from the FIFO. Because AUX1 cannot access FIFO, the AUX1 does not work under the AULP mode.
Data ready (DRDY) interrupt will not be generated either in h/w pins or in interrupt statues register.
External synchronization (MIPI I3C^{SM}) is not supported.

5.4 POWER CONSUMPTION FOR SOME COMMON USE CASES

To provide reference power consumptions for some very common use cases, 3 chips have been measured under room temperature. The table below shows the 3 chips average result. The numbers are not intended to be as specification.

Chip Condition		Idd (uA)
SLEEP	Accel and Gyro = Sleep	1.91
Combo LN 1.6KHz	Accel=LN, Gyro=LN, ODR=1.6KHz	407.30
Combo LP 50Hz	Accel=ULP, Gyro=LP, ODR=50Hz, Accel=4x, Gyro=10x	199.06
Combo LP 200Hz	Accel=ULP, Gyro=LP, ODR=200Hz, Accel=4x, Gyro=10x	284.45
ALN 1.6KHz	Accel=LN, Gyro=Sleep, ODR=1.6KHz	115.72
ALP 4x 50Hz	Accel=LP, Gyro=Sleep, ODR=50Hz, Accel=4x,	64.02
AULP 4x 50Hz	Accel=ULP, Gyro=Sleep, ODR=50Hz, Accel=4x,	13.38
AULP 1x 50Hz	Accel=ULP, Gyro=Sleep, ODR=50Hz, Accel=1x,	10.82
GLN 1.6KHz	Accel=Sleep, Gyro=LN, ODR=1.6KHz	354.46
GLP 10x 50Hz	Accel=Sleep, Gyro=LP, ODR=50Hz, Gyro=10x	194.77

Table 2. Power consumption for some common use cases

5.5 POWER MODES TRANSITIONS

The transitions between gyro and accel operation modes will be explained in this section.

Even there are two different interfaces (AP/AUX1), the sensor power-mode is unique, and the priority (highest is on left, lowest is on right) is:

Accel: LN > LP > ULP > OFF.
Gyro: LN > LP > STDBY > OFF.

This means that if an interface is set in LN while another is in LP, the resulting state for the sensor will be LN.

Because AUX1 have LN mode only, the sensor will be in LN state when AUX1 is enabled.

6 SELF-TEST

Self-test is a way to check mechanical and electrical integrity of the sensor without any physical movement.

ICM-45605 and ICM-45686 has self-test embedded in the eDMP ROM software and enables customer to perform it.

During self-test, the part should be static and without any movement. Any motion applied to the part will cause self-test to fail.

The self-test can be executed from UI and AUX1 interfaces.

6.1 REGISTER FIELD FOR SELF-TEST

6.1.1 Parameter registers

The register fields below are used to configure self-test.

BIT FIELD NAME	BANK, ADDRESS AND BIT FIELD	REGISTER NAME	VALUE (HEX) FOR ST	FUNCTIONALITY
STC_INIT_EN	IMEM_SRAM 0x38(0)	IMEM_SRAM_REG_56	1	1: Initializes self-test parameters
ST_ACCEL_EN	IMEM_SRAM 0x38(1)	IMEM_SRAM_REG_56	1	1: Enable accel self-test operation
ST_GYRO_EN	IMEM_SRAM 0x38(2)	IMEM_SRAM_REG_56	1	1: Enable gyro self-test operation
ST_ACCEL_LIMIT	IMEM_SRAM 0x39(4:2)	IMEM_SRAM_REG_57	7	Tolerated ratio for accelerometer 7: 50%
ST_GYRO_LIMIT	IMEM_SRAM 0x39(7:5)	IMEM_SRAM_REG_57	7	Tolerated ratio for gyroscope 7: 50%
ST_AVG_TIME	IMEM_SRAM 0x38(7) IMEM_SRAM 0x39(1:0)	IMEM_SRAM_REG_56 IMEM_SRAM_REG_57	5	Duration for self-test 5: 320ms
STC_PATCH_EN[11:0]	IMEM_SRAM 0x3C(7:0) IMEM_SRAM 0x3D(3:0)	IMEM_SRAM_REG_60 IMEM_SRAM_REG_61	0	Do not use patch mechanism
STC_DEBUG_EN[31:0]	IMEM_SRAM 0x40(7:0) IMEM_SRAM 0x41(7:0) IMEM_SRAM 0x42(7:0) IMEM_SRAM 0x43(7:0)	IMEM_SRAM_REG_64 IMEM_SRAM_REG_65 IMEM_SRAM_REG_66 IMEM_SRAM_REG_67	0	0 for standard operation

6.1.2 Control registers

BIT FIELD NAME	BANK, ADDRESS AND BIT FIELD	REGISTER NAME	VALUE (HEX) FOR ST	FUNCTIONALITY
SOFT_RST	User Bank 0 0x7F(1)	REG_MISC2	1	Triggers soft reset operation.
INT1_STATUS_RESET_DONE	User Bank 0 0x19(7)	INT1_STATUS0	-	This bit is set to 1 when reset interrupt is generated
EDMP_PRGRM_IRQ0_0/1[15:0]	IPREG_TOP1 0x4F (7:0), 0x50 (7:0)	EDMP_PRGRM_IRQ0_0/1	0x4000	Sets eDMP start address for IRQ0
EDMP_PRGRM_IRQ1_0/1[15:0]	IPREG_TOP1 0x51 (7:0), 0x52 (7:0)	EDMP_PRGRM_IRQ1_0/1	0x4004	Sets eDMP start address for IRQ1
EDMP_PRGRM_IRQ2_0/1[15:0]	IPREG_TOP1 0x53 (7:0), 0x54 (7:0)	EDMP_PRGRM_IRQ2_0/1	0x4008	Sets eDMP start address for IRQ2
EDMP_SP_START_ADDR[7:0]	IPREG_TOP1 0x55 (7:0)	EDMP_SP_START_ADDR	5	Sets eDMP stack address
FIFO_GSLEEP_SHARED_SRAM[1:0]	IPREG_TOP1 0xA7(1:0)	FIFO_SRAM_SLEEP	3	
TESTOPENTABLE	User Bank 0 0x73 (0)	REG_HOST_MSG	1	1: Enable test operation
INT_STATUS_MASK_PIN_SELFTEST _DONE	User Bank 0 0x3A(2)	INT_APEX_CONFIG1	0 / 1	0: Enable interrupt generation when self-test is done 1: Disable interrupt generation for self-test
INT_ON_DEMAND_PIN_2_DIS	IPREG_TOP1 0x73 (5)	STATUS_MASK_PIN_16_23	0	
EDMP_ENABLE	User Bank 0 0x2A (6)	EDMP_APEX_EN1	1	1: Enable eDMP operation
EMDP_ON_DEMAND_EN	User Bank 0 0x73 (5)	REG_HOST_MSG	1	
INT_STATUS_SELFTEST_DONE	User Bank 0 0x3C (2)	INT_APEX_STATUS1	-	This bit is set to 1 when self-test interrupt is generated

6.1.3 Result registers

BIT FIELD	BANK, ADDRESS AND BIT FIELD	REGISTER NAME	FUNCTIONALITY
AX_ST_PASS	IMEM_SRAM 0x44 (0)	IMEM_SRAM_REG_68	0: Accel x-axis self-test passed
AY_ST_PASS	IMEM_SRAM 0x44 (1)		0: Accel y-axis self-test passed
AZ_ST_PASS	IMEM_SRAM 0x44 (2)		0: Accel z-axis self-test passed
GX_ST_PASS	IMEM_SRAM 0x44 (3)		0: Gyro x-axis self-test passed
GY_ST_PASS	IMEM_SRAM 0x44 (4)		0: Gyro y-axis self-test passed
GZ_ST_PASS	IMEM_SRAM 0x44 (5)		0: Gyro z-axis self-test passed
ST_PASS	IMEM_SRAM 0x44 (6) IMEM_SRAM_0x44(7)		0: done 1: In progress 2:error

6.1.4 Procedure for self-test

Field Name	BANK, ADDRESS AND BIT FIELD	Register Name	Value (Hex)	Description
SOFT_RST	Bank 0 0x7F (1)	REG_MISC2	1	Do software reset
INT1_STATUS_RESET_DONE	Bank 0 0x19(7)	INT1_STATUS0	1	Read for value one
PRGM_STRT_ADDR_IRQ_0(7:0)	IPREG_TOP1 0x4F(7:0)	EDMP_PRGRM_IRQ0_0	0x00	LSB for Program Address 0
PRGM_STRT_ADDR_IRQ_0(15:8)	IPREG_TOP1 0x50(7:0)	EDMP_PRGRM_IRQ0_1	0x40	MSB for Program Address 0
PRGM_STRT_ADDR_IRQ_1(7:0)	IPREG_TOP1 0x51(7:0)	EDMP_PRGRM_IRQ1_0	0x04	LSB for Program Address 1
PRGM_STRT_ADDR_IRQ_1(15:8)	IPREG_TOP1 0x52(7:0)	EDMP_PRGRM_IRQ1_1	0x40	MSB for Program Address 1
PRGM_STRT_ADDR_IRQ_2(7:0)	IPREG_TOP1 0x53(7:0)	EDMP_PRGRM_IRQ2_0	0x08	LSB for Program Address 2
PRGM_STRT_ADDR_IRQ_2(15:8)	IPREG_TOP1 0x54(7:0)	EDMP_PRGRM_IRQ2_1	0x40	MSB for Program Address 2
EDMP_SP_START_ADDR	IPREG_TOP1 0x55(7:0)	EDMP_SP_START_ADDR	0x05	EDMP Start address
FIFO_GSLEEP_SHARED_SRAM	IPREG_TOP1 0xA7(1:0)	FIFO_SRAM_SLEEP	0x03	Power Up EDMP SRAM
STC_INIT_EN	IMEM_SRAM 0x38(0)	IMEM_SRAM_REG_56	0x01	Enable self-test
ST_ACCEL_EN	IMEM_SRAM 0x38(1)	IMEM_SRAM_REG_56	0x01	Enable self-test for Accel
ST_GYRO_EN	IMEM_SRAM 0x38(2)	IMEM_SRAM_REG_56	0x01	Enable self-test for Gyro
ST_ACCEL_LIMIT	IMEM_SRAM 0x39(4:2)	IMEM_SRAM_REG_57	0x07	Accel self-test limit 50%
ST_GYRO_LIMIT	IMEM_SRAM 0x39(7:5)	IMEM_SRAM_REG_57	0x07	Gyro self-test limit 50%
ST_AVG_TIME	IMEM_SRAM 0x38(7); 0x39(1:0)	IMEM_SRAM_REG_56 IMEM_SRAM_REG_57	0x05	Self-test average time 320msc
STC_PATCH_EN[11:0]	IMEM_SRAM 0x3C(7:0); 0x3D(3:0)	IMEM_SRAM_REG_60 IMEM_SRAM_REG_61	0x00	Do not use patch mechanism
TESTOPENTABLE	Bank 0 0x73(0)	REG_HOST_MSG	0x01	1: Enable test operation
INT_STATUS_MASK_PIN_SELFTEST_DONE	Bank 0 0x3A(2)	Int_Apex_Config1	0x0	Enable self-test done interrupt
INT_ON_DEMAND_PIN_2_DIS	IPREG_TOP1 0x73(5)	STATUS_MASK_PIN_16_23	0x0	Execute EDMP self-test.
EDMP_ENABLE	Bank 0 0x2A(6)	EDMP_APEX_EN1	0x01	
EDMP_ON_DEMAND_EN	Bank 0 0x73(5)	REG_HOST_MSG	0x01	
INT_STATUS_SELFTEST_DONE	Bank 0 0x3C(2)	INT_APEX_STATUS1		Check if self-test is done. See Note-1
INT_STATUS_MASK_PIN_SELFTEST_DONE	Bank 0 0x3a(2)	Int_Apex_Config1	0x01	Disable self-test done interrupt

Note-1: When running the self-test from AUX1 interface, the register INT_APEX_STATUS1 cannot be accessed. User must wait for a prescribed amount of time (ST_AVG_TIME) for the operation to be completed.

6.1.5 Self-test results

Field Name	BANK, ADDRESS AND BIT FIELD	Register Name	Value	Description
AX_ST_PASS	IMEM_SRAM 0x44(0)	IMEM_SRAM_REG_68	1/0	0 mean Ax self-test Passed 1 means Ax self-test Failed
AY_ST_PASS	IMEM_SRAM 0x44(1)		1/0	0 mean Ay self-test Passed 1 means Ay self-test Failed
AZ_ST_PASS	IMEM_SRAM 0x44(2)		1/0	0 mean Az self-test Passed 1 means Az self-test Failed

GX_ST_PASS	IMEM_SRAM 0x44(3)		1/0	0 mean Gx self-test Passed 1 means Gx self-test Failed
GY_ST_PASS	IMEM_SRAM 0x44(4)		1/0	0 mean Gy self-test Passed 1 means Gy self-test Failed
GZ_ST_PASS	IMEM_SRAM 0x44(5)		1/0	0 mean Gz self-test Passed 1 means Gz self-test Failed
ST_PASS	IMEM_SRAM 0x44 (6) IMEM_SRAM_0x44(7)		0/1/2	0: done 1: In progress 2:error

7 HOW TO USE EXTERNAL INPUT CLOCK

The CLKIN pin on ICM-45686 provides the ability to input an external clock. A highly accurate external clock may be used rather than the internal clocks sources if greater clock accuracy is desired. The external clock together with internal interpolator provide an accurate sensor data ODR. The highly accurate ODR will reduce sensor data integration errors.

7.1 CLKIN

External clock input supports highly accurate clock input from 20 kHz to 40 kHz. It is user's responsibility to ensure the external clock within the range.
The CLKIN is a digital input signal. Its Electrical Characteristics must meet the Digital Input specification in the datasheet.
The external source CLKIN is used to generate an internal ODR time base that replaces the internally generated tick at nominal 6.4 KHz. To achieve the same expected ODR nominal frequency, a CLKIN at 32.000 kHz is required. If the CLKIN frequency differs from the 32.000 kHz, the resulting ODR will be scaled accordingly with the ratio of $\mathbf{f_{CLKIN}}$/32kHz.
The TMST value in FIFO packet is measured using ICM-45686 internal clock source, not the external clock from CLKIN.

7.2 MULTIPLE DEVICES SYNC

In addition to the accurate ODR, another usage for the CLKIN is to sync multiple ICM-45686 devices data sampling. A re-align command (RTC_ALIGN = 1) allows synchronizing the phase of the multiple devices that use the same CLKIN. When the command is received, both the CLKIN high frequency counter and the ODR grid are safely reinitialized, in such a way that allows a perfect synchronization from the next tick.
The Figure 3 shows this sync process operation, where two sensors using the same CLKIN are synchronized with the rtc_align command (received on the red arrow).
To start the alignment, there must be at least one sensor enabled in ICM-45686 before issue write of RTC_ALIGN = 1.

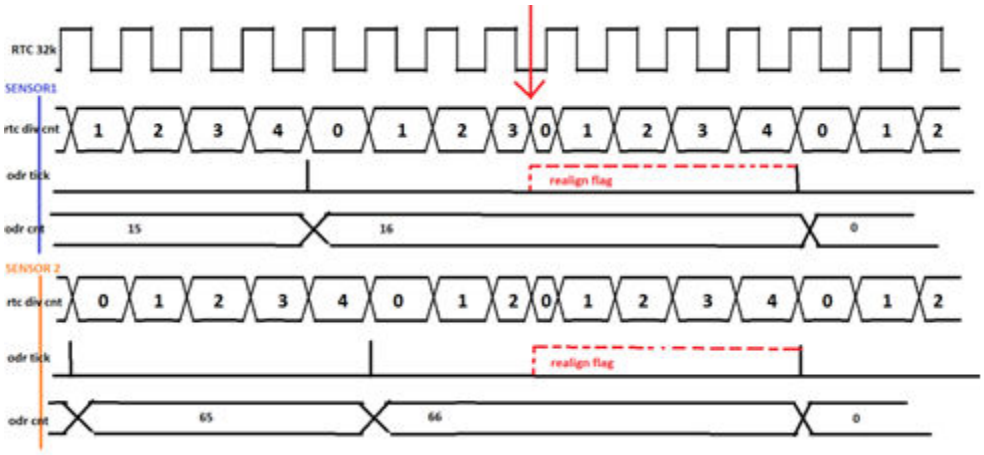


Figure 3. CLKIN sync process for two ICM-45686

7.3 CONFIGURATION REGISTER BIT FIELD

The CLKIN digital input is shared with other function signals on pin9. To use the pin9 as CLIKIN, the PADS_INT2_CFG_OVRD_VAL must be set to value 2.

PADS_INT2_CFG_OVRD bit must be set to 1 to allow the PADS_INT2_CFG_OVRD_VAL write.

Name: IOC_PAD_SCENARIO_OVRD
Bank: User bank 0
Address: 0x31

BIT	NAME	FUNCTION
2	PADS_INT2_CFG_OVRD	Override enable for PADS_INT2_CFG. 0: disable 1: enable
1:0	PADS_INT2_CFG_OVRD_VAL	Override value: Selects how pin 9 is used 0: INT2 is selected 1: FSYNC is selected 2: CLKIN is selected 3: Reserved

To enable the external CLKIN input function, the RTC_MODE bit must be set to 1.
As mentioned in the above, the multiple devices sync command can be issued when set RTC_ALIGN = 1.

Name: RTC_CONFIG
Bank: User bank 0
Address: 0x26

BIT	NAME	FUNCTION
6	RTC_ALIGN	RTC align bit. Re-align command is generated by writing 1 to this bit.
5	RTC_MODE	0: RTC functionality not enabled. 1: RTC functionality enabled. If also the I3C^{SM} Synchronous Mode functionality is enabled, then setting this bit to 1 will have no effect. RTC functionality can be enabled only if ACCEL_LP_CLK_SEL is set to 1; otherwise, device may not behave as expected.

Both I3C^{SM} STC and CLKIN use the same interpolator. I3C^{SM} STC has higher priority over the CLKIN. To use the CLKIN, user must disable the I3C^{SM} STC by setting the I3C_STC_MODE = 0;

Name: SIFS_I3C_STC_CFG
Bank: IPREG_TOP1
Address: 0x68

BIT	NAME	FUNCTION
2	I3C_STC_MODE	Enable the STC controller. 0: disable I3C^{SM} STC. 1: enable I3C^{SM} STC. Toggling this bit restarts the ODR frequency and phase correction operation as if the chip is out of reset. The STC functionality can be enabled only if accel_lp_clk_sel is set to 1; otherwise, device may not behave as expected.

Same as in I3C^{SM} STC mode, the ACCEL_SRC_CTRL[1:0] and GYRO_SRC_CTRL[1:0] must be set to 2'b10 (FIR and interpolator on).

Name: IPREG_SYS2_REG_123
Bank: IPREG_SYS2
Address: 0x7B

BIT	NAME	FUNCTION
1:0	ACCEL_SRC_CTRL[1:0]	SRC CTRL: 0: interpolator and FIR filter off, 1: interpolator off and FIR filter on, 2: interpolator on and FIR filter on, 3: reserved (debug mode).

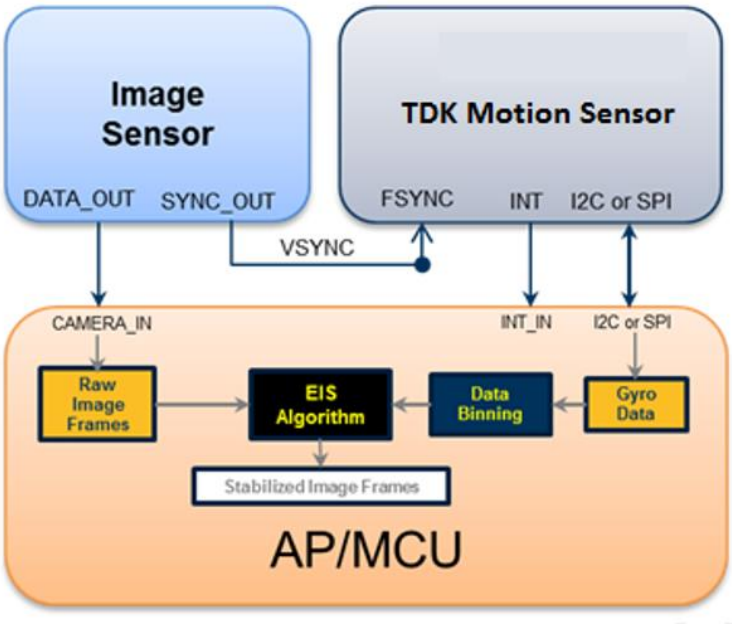
Name: IPREG_SYS1_REG_166
Bank: IPREG_SYS1
Address: 0xA6

BIT	NAME	FUNCTION
6:5	GYRO_SRC_CTRL[1:0]	SRC CTRL: 0: interpolator and FIR filter off, 1: interpolator off and FIR filter on, 2: interpolator on and FIR filter on, 3: reserved (debug mode).

8 FSYNC CONFIGURATION AND OPERATION

To achieve good video stabilization performance, video image frame needs to synchronize with motion sensor data. The video frame sync signal can be inputted to TDK IMU and be read out together with motion sensor data.

FSYNC is the input pin to the IMU chip which supports the function. The following block diagram illustrates how FSYNC should be connected.



The AP or MCU must associate gyro samples with the correspond frame. The image sensor sends the FSYNC pulse at the beginning of every frame to synchronize the gyro/accel data to the video frame. The AP or MCU post processes the image by reading image sensor frame(s) and gyro/accel data and associating the image frame with gyro/accel samples. For EIS, the result is an image stabilized frame. Inaccurate image-to-gyro/accel data alignment can result in image blur and jitter.

8.1 FSYNC DETECTION

There are three ways for FSYNC to be detected from host, and there are pros and cons for each method of them.

1. An interrupt can be triggered on an FSYNC event.
2. FSYNC bit can be polled on IMU sensor data LSB (temperature, gyro, or accelerometer data).
3. FSYNC information can be read from IMU FIFO data packet.

In the first 2 methods, in case system is too busy, host may not have time to read FSYNC information on time. In that case, it is difficult to know when the FSYNC signal happened. However, in method 3 all the data is stored in FIFO, including FSYNC flag and counter. It is then easy to find out during which gyro/accel data period FSYNC happened, even if the system is busy.

8.2 ALIGNMENT OF FSYNC AND SENSOR DATA

From motion sensor point of view, FSYNC input signal is asynchronous. Thus, a delta can exist between the FSYNC signal and the next gyro/accel sample.

In IMU devices, a FSYNC ODR Delay Counter stores the delta in µs between FSYNC signal and the first sensor data following FSYNC event. The host can read the delta from the FSYNC ODR Delay Counter and use this information to

create an interpolated gyroscope for EIS video stabilization. Interpolated sensor data has better alignment with FSYNC than original data resulting in more accurate EIS performance.

The FSYNC rising edge to the latest ODR delay is counted. The delay counter value is saved in FIFO data field or registers for user to read out.

The below figure illustrates the delay data.

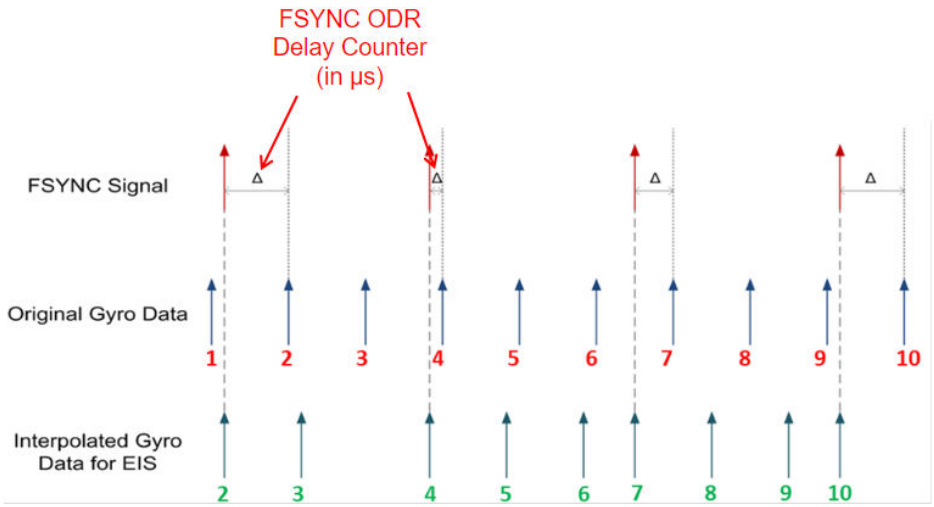


Figure 4. Timing Diagram

8.3 FSYNC CONFIGURATION (COMMON FOR FIFO MODE AND REGISTER MODE)

Name: SMC_CONTROL_0
Bank: User bank IPREG_TOP1
Address: 0x58

BIT	NAME	FUNCTION
1	TMST_FSYNC_EN	Time Stamp register FSYNC Enable. 0: Timestamp feature of FSYNC not enabled. 1: Timestamp feature of FSYNC enabled.

Name: INT1_CONFIG0
Bank: User bank 0
Address: 0x16

BIT	NAME	FUNCTION
4	INT1_STATUS_EN_AP_FSYNC	Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.

Name: INT1_STATUS0 Bank: User bank 0 Address: 0x19		
BIT	**NAME**	**FUNCTION**
4	INT1_STATUS_AP_FSYNC	Flags the occurrence of UI FSYNC event on INT1 0: Interrupt did not occur 1: Interrupt occurred

Name: INT2_CONFIG0 Bank: User bank 0 Address: 0x56		
BIT	**NAME**	**FUNCTION**
4	INT2_STATUS_EN_AP_FSYNC	Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.

Name: INT2_STATUS0 Bank: User bank 0 Address: 0x59		
BIT	**NAME**	**FUNCTION**
4	INT2_STATUS_AP_FSYNC	Flags the occurrence of UI FSYNC event on INT2 0: Interrupt did not occur 1: Interrupt occurred

8.4 FSYNC CONFIGURATION AND USE IN FIFO MODE

To use FSYNC feature in FIFO mode in optimal conditions, user should first:

- Configure and enable FIFO with gyro and accel during init time.
- Set gyro/accel FSR, ODR and power mode to appropriate values. To capture the full range of the movement that need to be compensated, it is advised to configure gyroscope in low-noise mode with FSR=500dps or higher and ODR=200Hz or faster.

The following registers are useful to configure and use FSYNC feature in FIFO mode:

Name: FIFO_CONFIG4 Bank: User bank 0 Address: 0x22		
BIT	**NAME**	**FUNCTION**
1	FIFO_TMST_FSYNC_EN	Enable the insertion of the Timestamp or FSYNC data into FIFO frame 0: No Timestamp/FSYNC data inserted into FIFO frame (timestamp fields are 0x0000). FSYNC_TAG_EN bit in FIFO header is 0. 1: Timestamp/FSYNC data inserted into FIFO frame. FSYNC_TAG_EN bit in FIFO header is set on an FSYNC trigger event.

FIFO header:

BIT	**NAME**	**FUNCTION**

2	FSYNC_TAG_EN	1: FSYNC is triggered and the Timestamp field contains the FSYNC-ODR delay 0: FSYNC is not triggered and the Timestamp field does not contain the FSYNC-ODR delay

Programming sequence:

- Set 1 in FIFO_TMST_FSYNC_EN
- Set 1 in TMST_FSYNC_EN

Once enabled, every FIFO packet corresponding to a FSYNC event would have its FSYNC flag set in FIFO header (FSYNC_TAG_EN=1) and FIFO timestamp field contains the FSYNC-ODR delay.

8.5 FSYNC CONFIGURATION AND USE IN REGISTERS MODE

To use FSYNC feature in registers mode in optimal conditions, user should first:

- Set gyro/accel FSR, ODR and power mode to appropriate values. To capture the full range of the movement that need to be compensated, it is advised to configure gyroscope in low-noise mode with FSR=500dps or higher and ODR=200Hz or faster.
- Set 1 in AP_FSYNC_FLAG_CLEAR_SEL, or AUX1_FSYNC_FLAG_CLEAR_SEL.
- Based on user tag selection, set tag FSYNC flag through registers AP_FSYNC_SEL[2:0] or AUX1_FSYNC_SEL[2:0]
- Set 1 in TMST_FSYNC_EN

Once enabled, after FSYNC pulse detected, the FSYNC-ODR delay data is saved to TMST_FSYNC_DATA_UI[15:0], or TMST_FSYNC_DATA_AUX1[15:0] for user to read out.

The following registers are used to configure FSYNC feature:

Name: FSYNC_CONFIG0
Bank: User bank 0
Address: 0x24

BIT	NAME	FUNCTION
3	AP_FSYNC_FLAG_CLEAR_SEL	Select the fsync flag clear policy 0 : the fsync flag is cleared when UI/AP sensor reg is updated 1 : the fsync flag is cleared when UI/AP serial interface reads the sensor register LSB of fsync tagged axis
2:0	AP_FSYNC_SEL[2:0]	Select the AP/UI sensor that will carry the FSYNC tagging. 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA_UI LSB 2: Tag FSYNC flag to GYRO_DATA_X_UI LSB 3: Tag FSYNC flag to GYRO_DATA_Y_UI LSB 4: Tag FSYNC flag to GYRO_DATA_Z_UI LSB 5: Tag FSYNC flag to ACCEL_DATA_X_UI LSB 6: Tag FSYNC flag to ACCEL_DATA_Y_UI LSB 7: Tag FSYNC flag to ACCEL_DATA_Z_UI LSB

Name: FSYNC_CONFIG1
Bank: User bank 0
Address: 0x25

BIT	NAME	FUNCTION
3	AUX1_FSYNC_FLAG_CLEAR_SEL	Select the AUX1 FSYNC flag clear policy. 0: The FSYNC flag is cleared when AUX1 sensor register is updated .

		1: The FSYNC flag is cleared when AUX1 serial interface reads the sensor register LSB of FSYNC tagged axis.
2:0	AUX1_FSYNC_SEL[2:0]	Select the AUX1 sensor that will carry the FSYNC tagging. 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA_AUX1 LSB 2: Tag FSYNC flag to GYRO_DATA_X_AUX1 LSB 3: Tag FSYNC flag to GYRO_DATA_Y_AUX1 LSB 4: Tag FSYNC flag to GYRO_DATA_Z_AUX1 LSB 5: Tag FSYNC flag to ACCEL_DATA_X_AUX1 LSB 6: Tag FSYNC flag to ACCEL_DATA_Y_AUX1 LSB 7: Tag FSYNC flag to ACCEL_DATA_Z_AUX1 LSB

Following registers are for FSYNC-ODR delay count. The delay can be read out from AP, or from AUX1 interface.

Name: TMST_FSYNCL
Bank: User bank 0
Address: 0x0F

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

Name: TMST_FSYNCH
Bank: User bank 0
Address: 0x0E

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

Name: TMST_FSYNCL_AUX1
Bank: User bank 0
Address: 0x53

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_AUX1[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

Name: TMST_FSYNCH_AUX1
Bank: User bank 0
Address: 0x52

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_AUX1[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

Programming sequence example

Configure/Enable FSYNC:

- Set 1 in AP_FSYNC_FLAG_CLEAR_SEL
- Set 1 in AP_FSYNC_SEL[2:0] (example here is Tag FSYNC to TEMP_DATA_UI LSB)
- Set 1 in TMST_FSYNC_EN

Once enabled, temperature register LSB would be set at each ODR following a FSYNC event. Then user should read FSYNC counter to get the delay between FSYNC event and current ODR event.

After each DRDY interrupt:

- Read fsync_flag = TEMP_DATA_UI[0] (read FSYNC flag in temperature data LSB)
- If fsync_flag is set:
    - read TMST_FSYNCL and TMST_FSYNCH (read 16b FSYNC counter)

When using FSYNC feature, the ODR frequency should be higher than FSYNC frequency. We suggest tagging FSYNC with the temperature LSB.

9 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
07/25/2024	1.0	Initial release

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